# Gabriele Formicone, PhD

EDUCATION: PhD in Electrical Engineering, Arizona State University (2001)
MS in Electrical Engineering, Arizona State University (1996)
Laurea in Physics, University of Rome "La Sapienza", Italy (1994)
Technology Entrepreneurship & Management certificate, ASU (2009)

PROFESSIONAL EXPERIENCE

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| 1/06 to present | Director of Technology and Innovation<br>Integra Technologies, Inc., www.integratech.com | |
| 5/15 to present | Faculty Associate, | Arizona State University, EE Dept. |
| 8/02 to 12/08 | Adjunct Faculty, | Mesa Community College |
| 6/97 to 12/05 | TCAD Device Simulation/Modeling Lead Engineer<br>Freescale Semiconductors, Tempe, AZ, USA | |
| 8/94 to6/97 | Research Assistant, | Arizona State University, Tempe, AZ, USA |

TEACHING EXPERIENCE

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|---|---|
| EEE202 | Circuits I |
| EEE241 | Fundamentals of Electromagnetics |
| EEE352 | Properties of Electronic Materials |

PATENTS

1) G. Formicone, *Transistor Including Shallow Trench and Electrically Conductive Substrate for Improved RF Grounding*, awarded in January 2013 (US 20120126243 A1).

## PUBLICATIONS

1) G. F. Formicone, D. Vasileska and D. K. Ferry, *2D Monte Carlo Simulation of Hole and Electron Transport in Strained Si,* Proceedings of the Fourth International Workshop on Comp. Electronics, 1996.
2) G. F. Formicone, D. Vasileska and D. K. Ferry, *Transport in the Surface Channel of Strained Si on a Relaxed $Si_{1-x}Ge_x$ Substrate,* Solid State Electronics 41, pp. 879-885, 1997.
3) G. F. Formicone, D. Vasileska and D. K. Ferry, *Modeling of Submicron $Si_{1-x}Ge_x$ based MOSFETs by Self-Consistent Monte Carlo Simulation,* Phys. Status Solidi (b) 204, pp. 531-533, 1997.
4) D. Vasileska , G. F. Formicone and D. K. Ferry, *Doping Dependence of the Mobility Enhancement in Surface-Channel Strained-Si Layer,* Proceedings of the Silicon Nanoelectronics Workshop, 1998.
5) D. K. Ferry, D. Vasileska and G. F. Formicone, *Carrier Transport and Velocity Overshoot in Strained Si on $Si_{1-x}Ge_x$ Heterostructures,* Material Research Society Spring meetings, special Symposium on Epitaxy and Applications of Si-based Heterostructures, April 13-15, 1998.
6) M. Saraniti, G. Zandler, G. F. Formicone, S. Wiggler and S. Goodnick, *Cellular Automata Simulation of nm-scale MOSFETs,* Semiconductor Science and Technology, 1997.
7) M. Saraniti, G. Zandler, G. F. Formicone and S. Goodnick, *Cellular Automata Studies of Vertical Silicon Devices,* Proceedings of the Fifth International Workshop on Comp. Electronics, 1997.
8) Formicone, G.F., Saraniti, M., Vasileska, D.Z., Ferry, D.K.; *Study of a 50 nm nMOSFET by ensemble Monte Carlo simulation including a new approach to surface roughness and impurity scattering in the Si inversion layer***,** IEEE Transactions on Electron Devices, Volume 49, Issue 1, Jan. 2002 pp: 125–132
9) Formicone, G.F., Saraniti M., Ferry, D.K.; *On the electron transient response in a 50nm MOSFET by Ensemble Monte Carlo Simulation in presence of the smoothed potential algorithm,* Journal of Computational Electronics, vol. 1, pp 251-255, 2002.

10) Burger, W., Ma, G., Dragon, C.; Formicone, G., Pryor, B., Ren, X.**,** *RF-LDMOS: A silicon-Based, High Power, High Efficiency Linear Power Amplifier Technology,* 2000 International Conference on Gallium-Arsenide MANufacturing TECHnology (MANTECH).
11) Brech, H.; Brakensiek, W.; Burdeaux, D.; Burger, W.; Dragon, C.; Formicone, G.; Pryor, B.; Rice, D.*; Record efficiency and gain at 2.1 GHz of high power RF transistors for cellular and 3G base stations*, IEDM '03 Technical Digest. 8-10 Dec. 2003
12) Burger, W., Brech, H., Burdeaux, D., Dragon, C.; Formicone, G., Honan, M., Pryor, B., Ren, X.**;** *RF-LDMOS: a device technology for high power RF infrastructure applications*; IEEE Compound Semiconductor Integrated Circuit Symposium, 2004.
13) Formicone, G.F.; Burger, W.; Pryor, B.; *Analysis of distributed multi-finger high-power transistors using the FDTD method*, IEEE MTT-IMS2005, Long Beach, CA, USA
14) Johnston JA, Formicone G, Hamm TM, Santello M.; *Assessment of across-muscle coherence using multi- vs. single- unit recordings*, Exp Brain Res. 2010 Dec; 207(3-4):269-82. doi: 10.1007/s00221-010-2455-4. Epub 2010 Nov 3.
15) Santello, M, Formicone, G; Johnston, JA; Hamm, TH; *Assessment of across-muscle coherence using multi- vs. single- unit signals*, Soc. Neurosci. Abst. 399.3 (2005).
16) Formicone, G.F.; Boueri, F.; Burger, J.; Cheng, W.; Kim, Y.; Titizian, J.; *RF LDMOS Power Transistor Technology for Pulsed L-band Transmitters*, white paper published in www.rfglobalnet.com.
17) Formicone, G.F.; Boueri, F.; Burger, J.; Cheng, W.; Kim, Y.; Titizian, J.; *Analysis of Bias Effects on VSWR Ruggedness in RF LDMOS for Avionics Applications*, European Microwave Week, 2008, Amsterdam, The Netherlands.
18) Formicone, G.F.; et al.; *Reduced Bias Depolarization Effects in Pulse Operated AlGaN/GaN HEMT on Silicon*, RADCOM-2011, Hamburg, Germany.
19) Formicone, G.F.; et al.; *A 130W LDMOS for 2.7-3.5GHz Broadband Radar Applications*, European Microwave Week, 2011, Manchester, UK.
20) J. Walker, G Formicone, F. Boueri, B. Battaglia; *A 1-KW S-Band GaN Radar Transistor*, IEEE COMCAS-2013, Israel.
21) J. Custer, G Formicone; *High Efficiency Switch Mode GaN-based Power Amplifiers for P-Band Aerospace Applications*, IEEE Aerospace Conference-2014, Montana, USA.
22) G Formicone, J. Custer; *Mixed-Mode Class E-F-1 High Efficiency GaN Power Amplifiers for P-Band Space Applications*, IEEE MTT-IMS2015, Phoenix, AZ, USA.
23) G Formicone, J. Custer; *Analysis of a GaN/SiC UHF Radar Power Amplifier for Operation at 125V Bias, European Microwave Week, 2015, Paris, France.*
24) G Formicone; *RF Burn-in Analysis of 100V P-Band Aerospace GaN Radar Transistors*, IEEE Aerospace Conference-2016, Montana, USA.
25) G Formicone et al.; *Targeting Radar with 150V RF GaN HEMTs*, Compound Semiconductor Magazine - March 2016, volume 22, issue 2.
26) G. Formicone, *Thermal Analysis of 100V GaN RF Transistors for CW High Power ISM Applications*, talk at IMAPS / RaMP, San Diego, March 2016
27) J. Custer, G. Formicone and J. L.B. Walker; *Recent Advances in kW-level Pulsed GaN Transistors with Very High Efficiency*, MRW2016 (International Conference on Microwave, Radar and Wireless Communications, Krakow, Poland, 2016).
28) G. Formicone et al.; *Quest for Vacuum Tubes' Replacement: 150V UHF GaN Radar Transistor,* European Microwave Week, 2016, London, UK
29) G. Formicone et al.; *Solid-State RF Power Amplifiers for ISM CW Applications Based on 100V GaN Technology*, European Microwave Week, 2016, London, UK
30) G. Formicone et al. *150 V-Bias RF GaN for 1 kW UHF Radar Amplifiers*, IEEE Compound Semiconductor Integrated Circuit Symposium, 2016, Austin, TX, USA.
31) G. Formicone et al.; *A UHF 1-kW Solid-State Power Amplifier for Spaceborne SAR*, IEEE / MTT-S PAWR-2017, Phoenix, AZ, USA
32) G. Formicone et al.; *A GaN Power Amplifier for 100 VDC Bus in GPS L-band*, IEEE / MTT-S PAWR-2017, Phoenix, AZ, USA
33) G. Formicone, J. Custer, and J. Burger; First Demonstration of a GaN-SiC RF Technology Operating Above 100 V in S-band; CS-MANTECH 2017, Indian Wells, CA, USA

34) F. Trevisan; A. Raffo; G. Bosi; V. Vadalà; G. Vannini; G. Formicone; J.Burger; J. Custer; *75-VDC GaN technology investigation from a degradation perspective*; 2017 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC) April 20-21, 2017, Graz, Austria
35) G. Formicone et al.; *Revisiting Power vs. Bandwidth in Broadband CW Amplifiers by Exploring 100 V Bias Operation*, European Microwave Week, 2017, Nuremberg, Germany
36) G. Bosi, A. Raffo, V. Vadalà, F. Trevisan, G. Formicone, J. Burger, J. Custer, G. Vannini; *Evaluation of High Voltage Transistor Reliability Under Nonlinear Dynamic Operation*; European Microwave Week, 2017, Nuremberg, Germany