David Antonio Zaragoza

dazarago@asu.edu • (928) 919-2981 • github.com/David-Zaragoza • linkedin.com/in/davidazaragoza

EDUCATION

Arizona State University, Tempe, AZ ***Expected May 2025***

Bachelor of Science in Engineering, Electrical Engineering

SKILLS

Hardware: PCB design, RTL/FPGA design, oscilloscope analysis, computer architecture, RF design, antenna design, mixed-signal design, physical circuit implementation, wiring, soldering

Software: LTSpice, Quartus Prime, SystemVerilog, C++, Python, Altium, Digital, Arduino, Office products, scripting

Interpersonal: Enterprise administration, interdisciplinary leadership, systems thinking, technical communication

WORK EXPERIENCE

Student Regent, Arizona Board of Regents, Phoenix, AZ ***July 2023 - Present***

- Appointed by Governor of Arizona with the consent of the State Senate to oversee Arizona's public university system, valued at **$11 billion**, serving **220,000 students** across **3 universities** and **25 campuses**.
- Approved creation of 4 new academic majors at Arizona State University, 2 university annual capital plans totalling at **more than $160 million**, and a capital improvement plan valued at **more than $450 million**.
- Collaborate with university presidents and senior leadership to implement new academic majors and medical schools.

Student Researcher, The Luminosity Lab, Tempe, AZ ***September 2021 - Present***

- Employ strategic design, systems thinking, and rapid prototyping to work with engineering, design, and business students to deploy solutions to complex interdisciplinary problems.
- *Reusable Washer Project*: Project commissioned by beverage distributor to reduce single-use cup waste. Programmed a servo linked to an **Arduino** microcontroller with **C++** to transport cups from a receiving receptacle to a sanitizing apparatus.

TECHNICAL PROJECTS

ARM Microprocessor

- Simulated a reduced instruction set ARM **computer architecture** on an Intel Cyclone V **FPGA** using **Quartus Prime**.
- Features include conditional logic, a controller, decoder, data memory, and instruction memory, all scripted in **SystemVerilog**.
- Wrote testbench script in **Python** and top-level module and logic component scripts in **System Verilog** for CPU.

RF Power Amplifier and Antenna

- Power amplifier designed with **Altium**. Operates at frequencies up to **6 GHz**, with a power output approximately above **10 dB**.
- Probe-fed patch antenna added on back layer through a via with a probe-coupled connection. Input impedance of 50 Ohms.
- Voltage-controlled oscillator managed by an **analog-to-digital converter**

Buck Converter

- DC-DC converter designed with **Altium**. Able to convert input voltages from **7V - 14V**, with an output voltage of **5V**, and an output current of **1A**.

Common Source, Gate, and Drain Amplifiers

- Simulated MOS amplifiers in **LTSpice**, obtaining signal source, output waveforms, and amplifier gains using transient analysis.
- Physically constructed amplifiers using discrete components, DC power sources, and function generators. Analyzed and recorded signal source and output voltage waveforms on **oscilloscopes**.
- Performed error analysis on simulated and measured results, comparing current and voltage values.

Generic 4-bit Microprocessor

- Thermostat chip architecture simulated using **logic design** with Java-based **Digital** software. Integrated components include multiplexers, decoders, and basic functions include and, not, or, and subtraction.

Digital Clock

- Created a clock with an **Arduino** Uno microcontroller programmed with **C++**, displaying time in *"12:00:00 AM"* format. Time is adjusted using two buttons, one which adjusts hours, the other which adjusts minutes.
- Integrated LCD with microcontroller and buttons on breadboard, **wiring** and **soldering** LCD pins.

ACTIVITIES

Secretary, SHPE de ASU, Tempe, AZ ***May 2022 - April 2023***

- Published a weekly newsletter using Mailchimp for 1000 subscribers about upcoming events and how to get involved.
- Created an automated attendance system for general body meetings using **Google Office** and **QR Tiger**. System used by 100 students biweekly.

Apprentice and Technical Lead, InterVarsity Christian Fellowship, Tempe, AZ ***May 2022 - Present***

- Managed slides for events hosting as many as 80 people detailing activities assisting others with their spiritual needs.