Arnab Acharya

Ph.D, Arizona State University

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Education

2021-present **Ph.D.**, *Department of Electrical Engineering*, **Arizona State University (ASU)**, *Tempe, AZ,USA*, **CGPA 4.00**

2017-2020 **M.S (by research)**, *Department of Electrical Engineering*, **Indian Institute Technology Kharagpur, (IIT - Kharagpur)** , *India*

2010–2014 **B. Tech**, *Department of Electrical Engineering*, **West Bengal University of Technology**, *Kolkata, India*

Technical Skills

- **Power Electronics:** DC-AC inverters, DC-DC converters, Sic, GaN, soft-switching.
- **PCB Design Software:** Altium Designer, OrCad Layout
- **Simulation Software :** PLECS, Cadence, MATLAB/SIMULINK, LTSpice
- **HIL platform :** RT Box, OPAL-RT
- **Programming Platform :** TI-C2000 launchpad, FPGA Xilinx Virtex-5
- **Programming Language :** Verilog, C

Job Experience

May–Aug 2023 **National Renewable Energy Laboratory (NREL)**

- *Graduate intern in the Electric Vehicle Grid Integration (EVGI) team.*
- Hands-on working experience with *real multi-chemistry battery stacks of LiFePO4 (LFP) and LiNiMnCoO2 (NMC)* battery cells connected in series-parallel combination used for EVs and Behind The Meter Storage (BTMS) systems.
- $100\ W$ Dual Active Bridge (DAB) converter-based active cell balancing techniques.

Feb.2020–July2021 **Mercedes-Benz Research & Development India (MBRDI)**

- *Engineer at MBRDI in the technical compliance management system (tCMS) team.*
- $7\ kW$ On Board Chargers (OBC) for EVs.
- Optimization of DC network to increase overall range of EVs.
- Technical compliance as per market-specific regulations and internal standards set by Mercedes-Benz authorities.

Research

Grid-forming inverters **Universal Interoperability for Grid-Forming Inverters (UNIFI) Consortium of National Renewable Energy Lab. (NREL),DOE**

Ph.D research – Working on high-power (10 kW) 3-phase SiC/IGBT-based inverter with THD$< 3\%$ for grid-forming applications and analysis of inverter performance under adverse grid conditions.

- Enhancing inverter stability under large grid transient with frequency deviation $\geq 1\ Hz\ (1.66\%)$.
- Fault and LVRT mitigation for PV inverters, IEEE – 2800.
- Soft switching topology for high power inverters to improve peak efficiency by $2-3\%$.
- TI–C2000 micro-controller coding (F28379D MCU).

DC-DC converter **Two-Stage Multi-Phase Converter for data-center application**

Master's thesis – Developed a re-configurable bus voltage architecture in a two-stage multi-phase buck converter for 48 V to point-of-load (PoL) applications using a bank of pre-charged switching capacitors. This configuration helped to achieve :

- 52% improvement in load transient and 42.85% improvement in reference transient performance.
- 33% reduction in output capacitor size maintaining efficiency at 89.2%.
- A **GaN** based 60W hardware prototype of a $48-1$ V data-center converter has been developed with **8-layer PCB** and tested.
- High frequency (100 MHz) mixed signal PCB has been developed for closed-loop implementation and interface with **FPGA** platform.

Isolated converter

- Worked on a 100 W Dual active bridge type converter with 200 kHz switching frequency for active cell balancing techniques for EV battery pack and behind-the-meter storage systems (BTMS).

Awards and Accolades

2024 Conducted **Professional Education Seminar** on "*PV inverter design - Topologies, Control and Sytem Considerations*" in **IEEE Applied Power Elecrtonic Conference (APEC),2024**, Long Beach, California, USA.

2019 **Best Presentation Award** in **IEEE Applied Power Elecrtonic Conference (APEC),2019**, Anaheim, California, USA, for presenting in lecture session - "*Converters for Data-centers*"

Patent and Publications Google Scholar

Patent [1] **A. Acharya**, V. Inder Kumar and S. Kapat, "A BUCK CONVERTER SYSTEM TO MITIGATE TRANSIENTS", Status – **Granted**, Indian patent number 504302 and application number 201931018283 [click here]

Journal [1] **A. Acharya**, V. Inder Kumar and S. Kapat, "Dynamic Bus Voltage Reconfiguration in a Two-Stage Multi-Phase Converter for Fast Transients," *IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE)*, vol. 9, no. 1, pp. 48-57, Feb. 2021. [click here]

Conference [1] **A. Acharya** and R. Ayyanar, "Dual-dVOC Based Controlled Negative Sequence Current Injection for Grid-Forming Inverters under Asymmetrical Grid Conditions," 2023 *IEEE Power & Energy Society General Meeting (PESGM)*, Orlando, FL, USA, 2023, pp. 1-5. [click here]

[2] **A. Acharya** and R. Ayyanar, "Enhancing Stability of dVOC Controlled Grid-Forming Inverters Under Large Grid Transients - A Power Angle Based Approach," 2023 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Nashville, TN, USA, 2023, pp. 803-808. [click here]

[3] H. Qamar, H. Qamar, **A. Acharya** and R. Ayyanar, "Smith Predictor Control for Dynamically Varying DC Link Voltage with 240° - Clamped Space Vector PWM in Hybrid Electric Traction Drives," 2022 *IEEE Transportation Electrification Conference and Expo (ITEC)*, 2022, Anaheim, CA, USA, 2022, pp. 1242-1247. [click here]

[4] S. Kapat, A. K. Singha and **A. Acharya**, "A Hardware-Enabled Tool for Nonlinear Analysis of Digitally Controlled High-Freq. DC-DC Converters," IECON 2022 - 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6. [click here]

[5] **A. Acharya**, V. I. Kumar and S. Kapat, "Dynamic Bus Voltage Configuration in a Two-Stage Multi-Phase Buck Converter to Mitigate Transients," 2019 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 496-501. [click here]

Service

Reviewing manuscripts for the following professional society's refereed journals:

- IEEE transactions on Power Electronics (TPEL)
- IEEE Journal of Emerging and Selected Topics in Industrial Electronics (JESTIE)
- IEEE transactions on Circuits and systems - II