BIOGRAPHICAL SKETCH

PERSONAL INFORMATION

NAME: Arindam Sanyal

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Office: Interdisciplinary Science and Technology Building IV, 555B

EDUCATION/TRAINING

Institution	Degree	Completion date	Field of Study
Jadavpur University, India	B.E	05/2007	Electronics and Tele-Communication Engineering
Indian Institute of Technology Kharagpur, India	M.Tech	05/2009	Electronics and Electrical Communication Engineering
University of Texas at Austin	Ph.D	12/2015	Electrical and Computer Engineering

PROFESSIONAL EXPERIENCE

Institution	Position	Dates
School of Electrical, Computer and Energy Engineering, Arizona State University	Assistant Professor	08/2021-Present
Department of Electrical Engineering, State University of New York	Assistant Professor	08/2016-07/2021
Silicon Laboratories, Austin, TX	Analog Design Engineer	06/2015-06/2016

RESEARCH INTERESTS

My research work lies at the convergence of circuit design and machine learning with applications in health-care, edge computing, high-energy physics, hardware security and electronic design automation. A major research focus of my group is developing on-chip analog AI circuits and sensors for personalized health monitoring, and we have developed several prototypes and validated some of them through small-scale human subject studies. In addition to health monitoring, these AI circuits also have applications in identifying new physics and reducing data volume in particle colliders. Another major research focus of my group is developing high-performance data converters from kHz-GHz speeds using novel time-domain signal processing techniques and AI for error calibration. My group is also designing ultra-low energy true random number generators and physical unclonable functions as examples of hardware security primitives. A significant part of my future research will be devoted to improving and expanding our AI classifier chips to incorporate other bio-markers and detect a wider variety of diseases as well as to collaboratively develop flexible wearables that will integrate our AI chips. Building upon our expertise in both integrated circuits design and AI, other research areas I want to explore are - a) develop AI-based frameworks for automated design of data converters and other mixed-signal circuits; b) AI-based compact transistor models for extreme conditions (deep cryogenic temperatures and high radiation doses) and develop data converters and timing circuits for these extreme conditions using our compact models.

SELECTED HONORS and AWARDS

1. Sony Faculty Innovation Award 2022.
2. ASU-Mayo Faculty Summer Residency Fellowship 2022.
3. Best Paper Award at IBM AI Compute Symposium 2020.
4. NSF CISE Research Initiation Initiative (CRII) Award, 2019 (supports early-career scientists within the first three years of their academic appointment and without prior federal award).
5. Buffalo Blue Sky Silver Coin Award, 2018, 2021 (awarded to top 4% faculties at State University of New York).
6. Intel/Texas Instruments/Catalyst Foundation CICC Student Scholarship Award, 2014.

PUBLICATIONS, INTELLECTUAL PROPERTY, AND PRESENTATIONS

SUMMARY OF PUBLICATIONS AND INTELLECTUAL PROPERTY
Total Journal Publications: # 45
Journal Publications from ASU: # 12
Journal Publications prior to ASU: # 33

Total Referred Conference Publications: # 56
Refereed Conference Publications from ASU: # 19
Refereed Conference Publications prior to ASU: # 37

Book Chapters Published: # 1
Intellectual Property: Patents # 4, Patents Pending #3

SUMMARY OF PRESENTATIONS
Invited Presentations - External: # 15
Invited Conference Presentations, including students: # 18
Refereed Conference Presentations, including students: #56

LEGEND

(*) Corresponding Author
Bold Font: ASU Ph.D. Student for whom Dr. Sanyal is the primary advisor
(X) ASU Postdoctoral Researcher
Bold Italic Font: SUNY Ph.D. Student for whom Dr. Sanyal is the primary advisor
(#) SUNY MS Student for whom Dr. Sanyal is the primary advisor
(~) Presenting author

JOURNAL PUBLICATIONS

1. **Jose Sanchez**, **Sumukh Bhanushali**, ***Sudarsan Sadasivuni***, Imon Banerjee, and Arindam Sanyal, "Low-Power Flexible Classifier Chip for Atrial Fibrillation Detection", *IEEE Transactions on Circuits and Systems for Artificial Intelligence (TCAS-AI)*, 2025.
2. Sanchari Das, Shruti Konwar, Sanjay Kumar, Arindam Sanyal and Bibhu Datta Sahoo, "An 8-bit Split CDAC-Based Noise-Shaping SAR ADC in 180 nm CMOS for Power Efficient Digitization of Sensor Signals", *IEEE Transactions on Instrumentation and Measurement,* 2025.
3. **Sumukh Prashant Bhanushali** and Arindam Sanyal, "A 13.2fJ/Step 74.3-dB SNDR Pipelined Noise-Shaping SAR+VCO ADC", *IEEE Open Journal of the Solid-State Circuits Society (OJ-SSCS),* 2024.
4. **Vasundhara Damodaran**, Ziyu Liu, Jian Meng, Jae-sun Seo, and Arindam Sanyal, "SRAM In-Memory Computing Macro With Delta-Sigma Modulator Based Variable-Resolution Activation", *IEEE Solid-State Circuits Letters*, 2023.
5. ***Sudarsan Sadasivuni***, Monjoy Saha, **Sumukh Prashant Bhanushali**, Imon Banerjee, and Arindam

Sanyal, "In-sensor artificial intelligence and fusion with electronic medical records for at-home monitoring", *IEEE Transactions in Bio-medical Circuits and Systems (TBioCAS)*, 2023.

6. ***Sudarsan Sadasivuni***, **Sumukh Bhanushali**, Imon Banerjee, and Arindam Sanyal, "In-sensor neural network for high energy efficiency analog-to-information conversion", *Scientific Reports, 2022*.
7. Amartya Bhattacharya, ***Sudarsan Sadasivuni***, Chieh-Ju Chao, Pradyumna Agasthi, Chadi Ayoub, David R Holmes, Reza Arsanjani, Arindam Sanyal, and Imon Banerjee, "Multi-modal fusion model for predicting adverse cardiovascular outcome post percutaneous coronary intervention", *Physiological Measurements, 2022.*
8. ***Sudarsan Sadasivuni***, Monjoy Saha, Neal Bhatia, Imon Banerjee and (*)Arindam Sanyal, "Fusion of Fully Integrated Analog Machine Learning Classifier with Electronic Medical Records for Real-time Prediction of Sepsis Onset", *Scientific Reports, 2022*.
9. ***Sanjeev Tannirkulam Chandrasekaran***, Abraham Peedikayil Kuruvila, Kanad Basu, and Arindam Sanyal, "Real-Time Hardware Based Malware and Micro-architectural Attack Detection Utilizing CMOS Reservoir Computing", *IEEE Transactions on Circuits and Systems-II,* vol. 69, no. 2*,* pp. 349-353, 2022*.*
10. Xiyuan Tang, Jiaxin Liu, Yi Shen, Shaolan Li, Linxiao Shen, Arindam Sanyal, Kareem Ragab and Nan Sun*,* "Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques"*, IEEE Transactions on Circuits and Systems-I,* vol. 69, no. 6, pp. 2249-2262, 2022*.*
11. ***Sanjeev Tannirkulam Chandrasekaran***, **Sumukh Prashant Bhanushali**, Imon Banerjee, and Arindam Sanyal, "Towards Real-Time, At-Home Patient Health Monitoring using Reservoir Computing CMOS IC", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 11, no. 4, pp. 829-839, 2021.
12. ***Sanjeev Tannirkulam Chandrasekaran***, **Sumukh P. Bhanushali**, Stefano Pietri, and Arindam Sanyal, "OTA-free 1-1 MASH ADC using Fully Passive Noise Shaping SAR & VCO ADC", *IEEE Journal of Solid-State Circuits*, pp. 1100-1111, vol. 57, no. 4, 2021.
13. ***Sanjeev Tannirkulam Chandrasekaran***, (#)Akshay Jayaraj, (#)Vinay Elkoori Ghantala Karnam, Imon Banerjee, and Arindam Sanyal, "Fully Integrated Analog Machine Learning Classifier Using Custom Activation Function for Low Resolution Image Classification", *IEEE Transactions on Circuits and Systems-I*, vol. 68, no. 3, pp. 1023-1033, 2021.
14. Junyu Lai, ***Sanjeev Tannirkulam Chandrasekaran***, Arindam Sanyal, and Jung-Hun Seo, "Flexible CMOS Chip Converted by A Novel Chip Transformation Process", *IET Electronics Letters*, vol. 56, no. 24, pp. 1335-1337, 2020.
15. ***Sanjeev Tannirkulam Chandrasekaran***, Stefano Pietri, and Arindam Sanyal, "21fJ/step OTA-Less, Mismatch-Tolerant Continuous-Time VCO-Based Band-Pass ADC", *IEEE Solid-State Circuits Letters (special section for ESSCIRC)*, vol. 3, pp. 342-345, 2020.
16. ***Sanjeev Tannirkulam Chandrasekaran***, **Sumukh Prashant Bhanushali**, Imon Banerjee, and Arindam Sanyal, "A Bio-Inspired Reservoir-Computer for Real-Time Stress Detection from ECG Signal", *IEEE Solid-State Circuits Letters (special section for ESSCIRC)*, vol. 3, pp. 290-293, 2020.
17. ***Mohammadhadi Danesh***, (#)Aishwarya Bahudhanam Venkatasubramaniyan, (#)Gaurav Kapoor, (#)Naveen Ramesh, ***Sudarsan Sadasivuni***, ***Sanjeev Tannirkulam Chandrasekaran***, and Arindam Sanyal, "Unified Analog PUF and TRNG based on Current Steering DAC and VCO", *IEEE Transactions on Very Large Scale Integration Systems*, vol. 28, no. 11, pp. 2280-2289, 2020.
18. ***Sanjeev Tannirkulam Chandrasekaran***, (#)Vinay Elkoori Ghantala Karnam, and Arindam Sanyal, "0.36mW, 52Mbps True Random Number Generator Based on a Stochastic Delta-Sigma Modulator", *IEEE Solid-State Circuits Letters (special section for ESSCIRC)*, vol. 3, pp. 190-193, 2020.
19. Shibo Zhou, Ying Chen, Xiaohua Li, and Arindam Sanyal, "Deep SCNN-based Real-time Object

Detection for Self-driving Vehicles Using LiDAR Temporal Data", *IEEE Access*, 2020.

20. ***Sanjeev Tannirkulam Chandrasekaran***, (#)Gaurav Kapoor, and Arindam Sanyal, "8fJ/step Bandpass ADC with Digitally Assisted NTF Re-configuration", *IEEE Transactions on Circuits and Systems-I,* vol. 67, no. 10, pp. 3262-3272, 2020.
21. ***Mohammadhadi Danesh***, and Arindam Sanyal, "0.13pW/Hz Ring VCO-Based Continuous-Time Read-Out ADC for Bio-Impedance Measurement", *IEEE Transactions on Circuits and Systems-II,* vol. 67, no. 12, pp. 2823-2827, 2020.
22. ***Sanjeev Tannirkulam Chandrasekaran***, (#)Ruobing Hua, Imon Banerjee, and Arindam Sanyal, "A Fully-Integrated Analog Machine Learning Classifier for Breast Cancer Classification", *MDPI Electronics,* vol. 9, no., 3, 2020.
23. Yanlong Zhang, Arindam Sanyal, Xueyi Yu, Xing Quan, Kailin Wen, Xiyuan Tang, Gang Jin, Li Geng, Nan Sun, "A Fractional-N PLL With Space-Time Averaging for Quantization Noise Reduction", *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 602-614, 2020.
24. (#)Akshay Jayaraj, (#)Nimish Nitin Gujarati, (#)Illakiya Venkatesh and Arindam Sanyal, "0.6V-1.2V, 0.22pJ/bit True Random Number Generator Based on SAR ADC", *IEEE Transactions on Circuits and Systems-II,* vol. 6, no. 10, pp. 1765-1769, 2020.
25. (#)Abilash Venkatesh, (#)Aishwarya Bahudhanam Venkatasubramaniyan, Xiaodan Xi, and Arindam Sanyal, "0.3pJ/bit Machine Learning Resistant Strong PUF using Subthreshold Voltage Divider Array", *IEEE Transactions on Circuits and Systems-II,* vol. 67, no. 8, pp. 1394-1398, 2020.
26. (#)Akshay Jayaraj, ***Mohammadhadi Danesh***, ***Sanjeev Tannirkulam Chandrasekaran***, and Arindam Sanyal, "76dB DR, 48fJ/step Second-Order VCO-Based Delta-Sigma Current-to-Digital Converter", *IEEE Transactions on Circuits and Systems-I,* vol. 67, no. 4, pp. 1149-1157, 2019.
27. Shaolan Li, Arindam Sanyal, Kyoungtae Lee, Yeonam Yoon, Xiyuan Tang, Yi Zhong, Kareem Ragab and Nan Sun, "Advances in Voltage-Controlled-Oscillator-Based ΔΣ ADCs", *ICICE Transactions on Electronics*, vol. 102, no. 7, pp. 509-519, 2019.
28. (#)Akshay Jayaraj, **Mohammadhadi Danesh**, **Sanjeev Tannirkulam Chandrasekaran**, and Arindam Sanyal, "Highly Digital Second-Order ΔΣ VCO ADC", *IEEE Transactions on Circuits and Systems-I, vol. 66, no. 7, pp. 2415-2425, 2019.*
29. (#)Akshay Jayaraj, **Sanjeev Tannirkulam Chandrasekaran**, (#)Archana Ganesh, Imon Banerjee, and Arindam Sanyal, "Maximum Likelihood Estimation based SAR ADC", *IEEE Transactions on Circuits and Systems-II*, vol. 66, no. 8, pp. 1311-1315, 2018.
30. **Sanjeev Tannirkulam Chandrasekaran**, (#)Akshay Jayaraj, **Mohammadhadi Danesh** and Arindam Sanyal, "Highly Digital Second-Order Oversampling TDC", *IEEE Solid-State Circuits Letters,* vol. 1, no. 5, pp. 114-117, 2018.
31. B. Ghanavati, E. Abiri, M. R. Salehi, A. Keyhani and A. Sanyal, "An Energy-Efficient SAR ADC with Lowest Total Switching Energy Consumption", *Analog Integrated Circuits and Signal Processing*, vol. *97, no. 1, pp. 123-133, 2018.*
32. B. Ghanavati, E. Abiri, M. R. Salehi, A. Keyhani and A. Sanyal, "LSB Split Capacitor SAR ADC with 99.2% Switching Energy Reduction", *Analog Integrated Circuits and Signal Processing,* vol. 93, no. 2, pp. 375-382, *2017.*
33. Imon Banerjee and (*)Arindam Sanyal, "Statistical estimator for simultaneous noise and mismatch suppression in SAR ADC", *Electronics Letters,* vol. 53, no. 12, pp. 6–8, 2017.
34. (*)Arindam Sanyal and Nan Sun, "An Energy-Efficient Hybrid SAR-VCO ΔΣ Capacitance-to-Digital Converter in 40nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 52, no. 7, pp. 1966–1976, 2017.
35. Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and Nan Sun, "A 0.7-V 0.6-uW

100-kS/s Low-Power SAR ADC With Statistical Estimation-Based Noise Reduction", *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1388–1398, 2017.

36. (*)Arindam Sanyal and Nan Sun, "A second-order VCO-based delta sigma ADC using a modified DPLL", *Electronics Letters,* vol. 52, no. 14, pp. 1204–1205, 2016.
37. Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and Nan Sun, "A 0.95-mW 6-b 700-Ms/s single-channel loop-unrolled SAR ADC in 40-nm CMOS", *IEEE Transactions on Circuits and Systems-II,* 2016.
38. (*)Arindam Sanyal, Xueyi Yu, Yanlong Zhang, and Nan Sun, "Fractional-N PLL with multi-element fractional divider for noise reduction", *Electronics Letters*, vol. 52, no. 10, pp. 809–810, 2016.
39. (*)Arindam Sanyal and Nan Sun, "Dynamic element matching techniques for static and dynamic errors in continuous-time multi-bit ΔΣ modulators", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS),* pp. 561–573, 2015.
40. (*)Arindam Sanyal, Long Chen, and Nan Sun, "Dynamic element matching with signal-independent element transition rates for multibit delta sigma modulators", *IEEE Transactions on Circuits and Systems–I,* pp. 1325–1334, May 2015.
41. Manzur Rahman, Arindam Sanyal, and Nan Sun, "A novel hybrid radix-3/radix-2 SAR ADC with fast convergence and low hardware complexity", *IEEE Transactions on Circuits and Systems–II,* pp. 426-430, May. 2015.
42. Kareem Ragab, Long Chen, Arindam Sanyal, and Nan Sun, "Digital background calibration for pipelined ADCs based on comparator decision time quantization", *IEEE Transactions on Circuits and Systems–II,* pp. 456-460, May. 2015.
43. (*)Arindam Sanyal, Peijun Wang and Nan Sun, "A thermometer-like mismatch shaping technique with minimum element transition activity for multi-bit delta-sigma DACs", *IEEE Transactions on Circuits and Systems–II*, pp. 461–465, 2014.
44. (*)Arindam Sanyal and Nan Sun, "An energy-efficient, low frequency-dependence switching technique for SAR ADC", *IEEE Transactions on Circuits and Systems–II,* pp. 294–298, 2014.
45. (*)Arindam Sanyal and Nan Sun, "A SAR ADC with 98% reduction in switching energy over conventional scheme", *Electronics Letters,* pp. 248–250, Feb 2013.

REFEREED CONFERENCE PUBLICATIONS

1. **(~)Tushar Gupta**, **Vasundhara Damodaran**, **Jose Sanchez**, and Arindam Sanyal, "Heart Abnormality Detection from Phonocardiogram Signals Using Reservoir Computing", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2025.
2. **(~)Tushar Gupta**, **Vasundhara Damodaran**, and Arindam Sanyal, "Reservoir Computing based AI for Estimating Remaining Useful Life of Turbofan Engine", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2025.
3. **(~)Jose Sanchez**, **Tushar Gupta**, **Vasundhara Damodaran**, Imon Banerjee, and Arindam Sanyal, "Prediction of Acute Kidney Injury Onset Using Electrocardiograph and Demographic Data Through Reservoir Computer On-Chip", *IEEE Biomedical Circuits and Systems Conference (BioCAS),* 2025.
4. **(~)Sumukh Prashant Bhanushali**, Debnath Maiti, Phaneendra Bikkina, Esko Mikkola and Arindam Sanyal, "Circuits-Informed Machine Learning Technique for Blind Open-Loop Digital Calibration of SAR ADC", *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2025.
5. **(~)Sumukh Prashant Bhanushali,** (X)Shamma Nasrin**,** and Arindam Sanyal, "Machine-learning based Blind Digital Calibration of Time-Interleaved ADC", *Special Sessions on IEEE VLSI Test Symposium (VTS),* 2025.

6. **(~)Matthew Kinsinger**, Anoop Bengaluru, Jia-Ching Chuang, **Sumukh Prashant Bhanushali**, Arindam Sanyal, "Mostly Digital, Calibration-Free, Band-Pass Delta-Sigma Modulator using Dual Time-Interleaved Noise-Shaping SAR ADCs", *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2025.
7. **(~)Jose Sanchez**, **Sumukh Prashant Bhanushali**, ***Sudarsan Sadasivuni***, Imon Banerjee, and Arindam Sanyal, "Mixed-Signal Classifier Chip on Flexible Substrate for Cardiovascular Health Monitoring", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2024.
8. **Vasundhara Damodaran**, **Jose Sanchez**, **(~)Tushar Gupta**, Phaneendra Bikkina, Esko Mikkola, Abdul-Muhsin Haidar, Imon Banerjee, and Arindam Sanyal, "AI-Enabled Fusion of Electrocardiograph and Demographics for Prediction of Acute Kidney Injury Onset", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2024.
9. **(~)Debnath Maiti, Sumukh Prashant Bhanushali**, and Arindam Sanyal, "Late Breaking Results: Machine Learning Based Reference Ripple Error Suppression in Successive Approximation Register Analog-to-Digital Converters", *Design Automation Conference (DAC),* 2024.
10. **(~)Sumukh Prashant Bhanushali, Tushar Gupta, Debnath Maiti,** and Arindam Sanyal, "Machine Learning Based Static and Dynamic Error Calibration in Data Converters", *Special Sessions on IEEE VLSI Test Symposium (VTS),* 2024.
11. **(~)Sumukh Prashant Bhanushali**, and Arindam Sanyal, "Enhancing Performance of SAR ADC Through Supervised Machine Learning", *IEEE International Symposium on Circuits and Systems (ISCAS*) 2024.
12. **(~)Sumukh Prashant Bhanushali**, ***Sudarsan Sadasivuni***, **Jose Sanchez**, Imon Banerjee, and Arindam Sanyal, "Fully Integrated Mixed-Signal Classifier for Cardiovascular Health Monitoring", *IEEE Biomedical Circuits and Systems Conference (BioCAS)* 2023.
13. **(~)Vasundhara Damodaran**, Ziyu Liu, Jae-sun Seo, and Arindam Sanyal, "A Delta-Sigma Based SRAM Compute-in-Memory Macro for Human Activity Recognition", *IEEE Biomedical Circuits and Systems Conference (BioCAS)* 2023.
14. **(~)Sumukh Prashant Bhanushali** and Arindam Sanyal, "A 13.2fJ/Step 74.3-dB SNDR Pipelined Noise-Shaping SAR+VCO ADC", *IEEE European Solid-State Circuits Conference (ESSCIRC)*, 2023.
15. **(~)Vasundhara Damodaran**, Ziyu Liu, Jae-sun Seo, and Arindam Sanyal, "A 138-TOPS/W Delta-Sigma Modulator-Based Variable-Resolution Activation In-Memory Computing Macro", *IEEE Custom Integrated Circuits Conference (CICC)*, 2023.
16. **(~)*Sudarsan Sadasivuni***, **Sumukh Prashant Bhanushali**, Imon Banerjee, and Arindam Sanyal, "A 43.6 TOPS/W AI Classifier with Sensor Fusion for Sepsis Onset Prediction", *IEEE Biomedical Circuits and Systems Conference (BioCAS),* 2022.
17. **(~)*Sudarsan Sadasivuni***, **Vasundhara Damodaran**, Imon Banerjee, and Arindam Sanyal, "Real-time prediction of cardiovascular diseases using reservoir-computing and fusion with electronic medical record", *IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS)* 2022.
18. **(~)*Sudarsan Sadasivuni***, Monjoy Saha, **Sumukh Prashant Bhanushali**, Imon Banerjee, and Arindam Sanyal, "Real-Time Sepsis Prediction Using Fusion of on-Chip Analog Classifier and Electronic Medical Record", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2022.
19. **(~)*Sudarsan Sadasivuni***, **Sumukh Prashant Bhanushali**, Sai S. Singamsetti, Imon Banerjee, and Arindam Sanyal, "Multi-Task Learning Mixed-Signal Classifier for In-situ Detection of Atrial Fibrillation and Sepsis", *IEEE Biomedical Circuits and Systems Conference (BioCAS),* 2021.
20. **(~)*Sanjeev Tannirkulam Chandrasekaran***, Imon Banerjee, and Arindam Sanyal,"7.5nJ/inference CMOS Echo State Network for Coronary Heart Disease prediction", *IEEE European Solid-State Circuits Conference (ESSCIRC),* 2021.

21. **(~)*Sanjeev Tannirkulam Chandrasekaran***, **Sumukh Prashant Bhanushali**, Stefano Pietri, and Arindam Sanyal, "OTA-free 1-1 MASH ADC using Fully Passive Noise Shaping SAR & VCO ADC", *IEEE Symposia on VLSI Technology and Circuits (VLSI-C),* 2021.

22. **(~)*Sudarsan Sadasivuni***, Rahul Chowdhury, (#)Vinay E. G. Karnam, Imon Banerjee, and Arindam Sanyal, "Recurrent Neural Network Circuit for Automated Detection of Atrial Fibrillation from Raw ECG", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2021.

23. **(~)*Sanjeev Tannirkulam Chandrasekaran***, (#)Akshay Jayaraj, (#)Naveen Ramesh, and Arindam Sanyal, "33-200Mbps, 3pJ/Bit True Random Number Generator Based on CT Delta-Sigma Modulator", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2021.

24. **(~)**Shibo Zhou, Xiaohua Li, Ying Chen, ***Sanjeev Tannirkulam Chandrasekaran***, and Arindam Sanyal, "Temporal-Coded Deep Spiking Neural Network with Easy Training and Robust Performance", *35th AAAI Conference on Artificial Intelligence, (AAAI-21)*, 2021.

25. **(~)*Sudarsan Sadasivuni***, ***Sanjeev Tannirkulam Chandrasekaran***, and Arindam Sanyal, "Neural Networks for Authenticating Integrated Circuits Based on Intrinsic Nonlinearity", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2020.

26. **(~)Sumukh Prashant Bhanushali**, ***Sudarsan Sadasivuni***, Imon Banerjee, and Arindam Sanyal, "Digital Machine Learning Circuit for Real-Time Stress Detection from Wearable ECG Sensor", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2020.

27. **(~)*Sanjeev Tannirkulam Chandrasekaran***, and Arindam Sanyal, "Stochastic Delta-Sigma VCO-ADC Utilizing 4x Staggered Averaging", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2020.

28. **(~)** (#)Akshay Jayaraj, Abhijit Das, (#)Srinivas Arcot and Arindam Sanyal, "8.6fJ/Step VCO-Based CT 2nd-Order Delta Sigma ADC", *IEEE Asian Solid-State Circuits Conference (A-SSCC),* 2019.

29. **(~)** (#)Ruobing Hua and Arindam Sanyal, "39fJ Analog Artificial Neural Network for Breast Cancer Classification in 65nm CMOS", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2019.

30. **(~)*Sanjeev Tannirkulam Chandrasekaran*** and Arindam Sanyal, "A Single Channel Bandpass SAR ADC with Digitally Assisted NTF Re-Configuration", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2019.

31. **(~)*Sanjeev Tannirkulam Chandrasekaran*** and Arindam Sanyal, "A Highly Digital VCO-Based Asynchronous Analog-to-Time Converter", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2019.

32. **(~)*Mohammadhadi Danesh*** and Arindam Sanyal, "Fully Digital 1-1 MASH VCO-Based ADC Architecture", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2019.

33. ***Mohammadhadi Danesh***, (#)Aishwarya Bahudhanam, (#)Gaurav Kapoor and Arindam Sanyal, "A 0.36pJ/Bit Analog PUF Based on Current Steering DAC and VCO", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2019.

34. **(~)** (#)Abilash Venkatesh and Arindam Sanyal, "A Machine Learning Resistant Strong PUF using Subthreshold Voltage Divider Array in 65nm CMOS", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2019.

35. **(~)** (#)Akshay Jayaraj, Imon Banerjee, and Arindam Sanyal, "Common-Source Amplifier Based Analog Artificial Neural Network Classifier", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2019.

36. **(~)** (#)Akshay Jayaraj, ***Mohammadhadi Danesh***, ***Sanjeev Tannirkulam Chandrasekaran*** and Arindam Sanyal, "0.43nJ, 0.48pJ/step Second-Order $\Delta\sum$ Current-to-Digital Converter for IoT Applications", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2019.

37. **(~)*Mohammadhadi Danesh***, (#)Akshay Jayaraj, ***Sanjeev Tannirkulam Chandrasekaran*** and Arindam Sanyal, "Ultra-Low Power Analog Multiplier Based on Translinear principle", *IEEE International Symposium on Circuits and Systems (ISCAS)* 2019.

38. **(~)**Yanlong Zhang, Arindam Sanyal, Xing Quan, Kailin Wen, Xiyuan Tang, Gang Jin, Li Geng and Nan Sun, "A 2.4-GHz ΔΣ Fractional-N Synthesizer with Space-Time Averaging for Noise Reduction", *IEEE Custom Integrated Circuits Conference* (CICC), 2019.

39. **(~)*Mohammadhadi Danesh***, ***Sanjeev Tannirkulam Chandrasekaran*** and Arindam Sanyal, "Ring Oscillator Based Delta-Sigma ADCs", *IEEE International Conference on Electronics, Circuits and Systems (ICECS),* 2018.

40. **(~)**Yi Zhong, Shaolan Li, Arindam Sanyal, Xiyuan Tang, Linxiao Shen, Siliang Wu, Nan Sun, "A Second-Order Purely VCO-Based CT ΔΣ ADC Using a Modified DPLL in 40-nm CMOS", *IEEE Asian Solid-State Circuits Conference (A-SSCC),* 2018.

41. **(~)*Sanjeev Tannirkulam Chandrasekaran*** and Arindam Sanyal, "A Digital PLL Based 2nd-Order ΔΣ Bandpass Time-Interleaved ADC", *IEEE MWSCAS,* 2018.

42. **(~)** (#)Aishwarya Bahudhanam and Arindam Sanyal, "Physically Unclonable Functions Based on Voltage Divider Arrays in Subthreshold Region", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

43. (~)Arindam Sanyal, Shaolan Li and Nan Sun, "Low-power Scaling-friendly Ring Oscillator based ΔΣ ADC", *IEEE International Symposium on Circuits and Systems (ISCAS),* 2018.

44. **(~)**Vaishak Prathap, ***Sanjeev Tannirkulam Chandrasekaran***, and Arindam Sanyal, "2nd-Order VCO-Based CT ΔΣ ADC Architecture", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018.

45. (~)Arindam Sanyal and Nan Sun, "A 18.5 fJ/step VCO-Based 0-1 MASH ΔΣ ADC with Digital Background Calibration", *IEEE Symposia on VLSI Technology and Circuits (VLSI-C)*, 2016.

46. **(~)**Long Chen, Arindam Sanyal, Ji Ma, and Nan Sun, "Comparator common-mode variation effects analysis and its application in SAR ADCs,", *IEEE International Symposium on Circuits and Systems (ISCAS),* 2016.

47. (~)Arindam Sanyal and Nan Sun, "A 55fJ/conv-step VCO-Based ΔΣ Capacitance-to-Digital Converter in 40nm CMOS", *IEEE European Solid-State Circuits Conference (ESSCIRC),* 2016.

48. **(~)**Long Chen, Xiyuan Tang, Arindam Sanyal, Yeonam Yoon, Jie Cong, and Nan Sun, "A 10.5-b ENOB 645nW 100kS/s SAR ADC with Statistical Estimation Based Noise Reduction", *IEEE Custom Integrated Circuits Conference (CICC)*, 2015.

49. (~)Arindam Sanyal, Kareem Ragab, Long Chen, T. R. Viswanathan, Shouli Yan and Nan Sun, "A hybrid SAR-VCO ΔΣ ADC with first-order noise shaping", *IEEE Custom Integrated Circuits Conference (CICC),* 2014.

50. **(~)**Long Chen, Arindam Sanyal, Ji Ma and Nan Sun, "A 24-uW 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique", *IEEE European Solid-State Circuits Conference (ESSCIRC),* 2014.

51. (~)Arindam Sanyal and Nan Sun, "An enhanced ISI shaping technique for multi-bit delta sigma DACs", *IEEE International Symposium on Circuits and Systems (ISCAS),* 2014.

52. (~)Arindam Sanyal and Nan Sun, "A low frequency-dependence, energy-efficient switching technique for bottom-plate sampled SAR ADC", *IEEE International Symposium on Circuits and Systems (ISCAS),* 2014.

53. (~)Arindam Sanyal and Nan Sun, "A very high energy-efficiency switching technique for SAR ADCs", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS),* 2013.

54. **(~)**Wenjuan Guo, Youngchun Kim, Arindam Sanyal, Ahmed Tewfik, and Nan Sun, "A single SAR ADC converting multi-channel sparse signals", *IEEE International Symposium on Circuits and Systems (ISCAS),* 2013.
55. (~)Arindam Sanyal and Nan Sun, "A Simple and Efficient Dithering Method for Vector Quantizer Based Mismatch-Shaped Delta Sigma DACs ", *IEEE International Symposium on Circuits and Systems (ISCAS),* 2012.
56. (~)Arindam Sanyal and Tarun Kanti Bhattacharyya, "Maximizing the sequence length in a MASH Delta Sigma Modulator by dithering", *IEEE MTT-S International Microwave Symposium (IMS),* 2009.

ABSTRACTS

1. **(~)*Sudarsan Sadasivuni***, **Vasundhara Damodaran**, Imon Banerjee, and Arindam Sanyal, "Real-time prediction of cardiovascular disease using fusion of electronic medical record and electrocardiogram", *AMIA Clinical Informatics Conference*, 2022.
2. **(~)*Sudarsan Sadasivuni***, Monjoy Saha, **Sumukh Prashant Bhanushali**, Imon Banerjee, and Arindam Sanyal, "Real-time sepsis prediction using fusion of on-chip analog classifier and electronic medical record", *IBM/IEEE-AI Compute Symposium,* 2021.
3. **(~)*Sanjeev Tannirkulam Chandrasekaran***, **Sumukh Prashant Bhanushali**, Imon Banerjee, and Arindam Sanyal, "Towards intelligent wearable health monitors using reservoir computing CMOS IC", *IBM/IEEE-AI Compute Symposium,* 2020.

BOOK CHAPTERS

1. Arindam Sanyal, Wenjuan Guo, and Nan Sun, "Hybrid VCO Based 0-1 MASH and Hybrid $\Delta\sum$ SAR", Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design, Springer, pp.61--67, 2018.

PATENTS

1. "Delta-sigma modulator enabled variable-input resolution in-memory computing SRAM macro", US patent #18/637,823.
2. "Analog-To-Digital Converter (ADC) Architectures for High Resolution and Energy Efficiency", US patent # 18/490,931.
3. "Machine Learning Enhanced Analog-to-Digital Converters", US patent application #19/051,527.
4. "On-chip Hyperdimensional computing using mixed-signal circuits", US patent application, #19/062,650.
5. "Deep neural network-based blind digital calibration of analog-to-digital converters without retraining", provisional US patent application. #63/919,324.
6. "Methods and related aspects for producing analog to digital circuit design", provisional US patent application. #63/837,259.
7. "Negative Miller capacitance assisted precision amplifier with correlated level shifting", provisional US patent application. #63/879,835.

INVITED PRESENTATIONS

1. ***Title:*** "Mixed-Signal Techniques for Remote Patient Monitoring with Intelligent Wearables", ***Location:*** NXP Distinguished Lecture Series, 2025.
2. ***Title:*** "Novel Design Techniques for High-Speed and Radiation-Hardened ADCs", ***Location:*** TSMC 2025.
3. ***Title:*** "On-chip Analog Reservoir Computing for Edge AI", ***Location:*** Semiconductor Research Corporation e-Workshop 2025.
4. ***Title:*** "Health management using intelligent wearables with mixed-signal AI", ***Location:*** Cirrus Logic, Chandler, AZ 2025.
5. ***Title:*** "Machine Learning Techniques for Health Management and Enhancing Circuit Performance", ***Location:*** University of Hawaii, 2025.
6. ***Title:*** "Enhancing performance of data converters through digital techniques and circuits-informed machine learning", ***Location:*** Oregon State University, 2025.
7. ***Title:*** "Health management using intelligent wearables with mixed-signal AI", ***Location:*** IEEE Workshop Austin, TX, 2024.
8. ***Title:*** "Enhancing performance of data converters using AI", ***Location:*** Cirrus Logic, Mesa, AZ 2023.
9. ***Title:*** "Analog TinyML for health management using intelligent wearables", ***Location:*** TinyML Phoenix Chapter, 2022.
10. ***Title:*** "Mostly Digital Delta-Sigma ADCs for High Energy Efficiency Data Conversion", ***Location:*** Cirrus Logic, Mesa, AZ 2022.
11. ***Title:*** "Voltage Controlled Ring Oscillators for High Energy Efficiency Data Conversion", ***Location:*** Global Conference on Semiconductors, Optoelectronics and Nanostructures, 2022.
12. ***Title:*** "Towards Personalized, At-Home Health Monitoring Using Intelligent Wearables", ***Location:*** SEMICON West, San Francisco CA 2021.
13. ***Title:*** "Low-power Mostly Digital Time-Domain Delta-Sigma ADCs for IoT", ***Location:*** Semiconductor Research Corporation e-Workshop 2020.
14. ***Title:*** "Mixed-Signal Circuit Design Methodologies for High Energy-Efficiency Computations", ***Location:*** Indian Institute of Sciences, Bangalore, India, Fall 2020.
15. ***Title:*** "Analog/Mixed-Signal Techniques for Machine Learning on Si", ***Location:*** IDEXBiometrics, Rochester, NY 2020.
16. ***Title:*** "Low Power Time-Domain ADCs", ***Location:*** IDEXBiometrics, Rochester, NY 2017.
17. ***Title:*** "VCO based $\Delta\sum$ADCs", ***Location:*** Cirrus Logic, Austin, TX 2016.
18. ***Title:*** "Building the Next Generation Time Domain Analog-to-Digital Converters", ***Location:*** Institute for Applied Mathematics and Information Technologies (IMATI), Italy 2015.

PERSONNEL: STUDENT SUPERVISION / MENTORING, TEACHING, DISSERTATION COMMITTEES, RESEARCHERS, AND OUTREACH

SUMMARY OF MENTORING (including co-mentored personnel):
Postdoctoral Researchers: 2
Ph.D. Students Graduated: 5 (2 at ASU, 3 at SUNY)
Ph.D. Students Current: 7
M.S. Thesis Students Graduated: 14 (1 at ASU, 13 at SUNY)
M.S. Project Students Current: 4
Undergraduate Students (Research): 3
Student Fellowships and Awards: 11

SUMMARY OF TEACHING:
Undergraduate Courses Taught, including New Course Development: 3 (2 at ASU with 3 sections of 335 and 4 sections of 433, 1 at SUNY with 4 sections of 491)
Graduate Courses Taught, including New Course Development: 3 (2 at ASU with 5 sections of 591 and 2 sections of 527, 1 at SUNY with 5 sections of 559)
Average Teaching Evaluation Score for Undergraduate Courses taught at ASU: 4.2* (In-person: 4.5/Online: 4.1)
Average Teaching Evaluation Score for Graduate Courses taught at ASU: 4.0* (In-person: 4.5/Online: 3.7)

*calculated using weighted averages from Fall 2021-Fall 2024

POST-DOCTORAL SCHOLARS CURRENT

1. **Shamma Nasrin:** Shamma received her PhD from University of Illinois, Chicago and started as post-doc in Fall 2024. She is leading projects on machine learning based calibration techniques for advanced data converters for ME Commons project as well as working on AI-based automation of data converter design.

2. **Saurabh Dhiman:** Saurabh received his PhD from The Indian Institute of Technology and started as post-doc in Fall 2024. He is working on radiation-hardened data converter design for ME Commons project.

DOCTORAL STUDENTS CURRENT

1. **Matthew Kinsinger:** Matthew started his PhD in Fall 2023. His research is on high-speed data converters. He has cleared his qualifying exam, has already taped-out 1 chip and working on his next chip tape-out. He has a first author paper in IEEE Radio Frequency Integrated Circuits Symposium (RFIC).

2. **Tushar Gupta:** Tushar started his PhD in Fall 2023. His research focus is on designing analog machine learning systems. He has authored/co-authored 2 papers in IEEE VLSI Test Symposium (VTS), IEEE Biomedical Circuits and Systems (BioCAS).

3. **Jose Sanchez:** Jose started his PhD in Fall 2023. His research focus is on machine learning circuits design for health monitoring. He has authored 3 papers including first author paper in IEEE Biomedical Circuits and Systems (BioCAS.

4. **Jie Fu**: Jie started her PhD in Fall 2024. Her research focus is on GHz speed data converters.

5. **Zuwei Guo**: Co-chair of Zuwei's doctoral committee. His research is on computer vision and electronic design automation using AI.

6. **Vincent Chuang:** Vincent started his PhD in Fall 2025. His research focus is on power management circuits.

7. **Qitong Zhu**: Qitong started his PhD in Fall 2025. His research focus is on high-resolution delta-sigma modulators.

DOCTORAL STUDENTS GRADUATED (AT ASU)

1. **Vasundhara Damodaran:** Vasundhara completed her PhD in Spring 2025. She has authored/co-authored 5 papers including first-author papers in IEEE Solid-State Circuits Letters and IEEE Custom Integrated Circuits Conference (CICC) which are top journals/conferences in solid-state circuits field. Her research focus is on custom mixed-signal accelerators for neuromorphic computing. ***Thesis topic***: Analog AI solutions for data deluge. She is currently with Intel, Oregon.

2. **Sumukh Prashant Bhanushali:** Sumukh completed his PhD in Spring 2025. He has authored/co-authored 20 journal and conference, with first-author papers in leading journals and conferences, such as IEEE Open Journal of the Solid-State Circuits Society (O-JSSCS), IEEE European Solid-State Circuits (ESSCIRC), IEEE Radio Frequency Integrated Circuits Symposium (RFIC) and IEEE Biomedical Circuits and Systems (BioCAS). ***Thesis topic:*** Improving SAR ADC performance with scaling friendly solutions. He will continue as post-doc in our group.

DOCTORAL STUDENTS GRADUATED (AT SUNY)

1. **Sudarsan Sadasivuni:** Sudarsan received his PhD in Spring 2022 and authored/co-authored 12 journal and conference publications including first-author publications in Nature Scientific Reports and IEEE Transactions on Biomedical Circuits and Systems (TBioCAS). ***Thesis topic:*** On-chip ultra-low power machine learning classifiers for continuous health monitoring. He is currently with Altera, AZ.

2. **Sanjeev Tannirkulam Chandrasekaran:** Sanjeev received his PhD in Spring 2021 and authored/co-authored 28 journal and conference publications including first-author publications in premier journal like IEEE Journal of Solid-State Circuits (JSSC), IEEE Symposia on VLSI Technology and Circuits (VLSI-C) and IEEE European Solid-State Circuits Conference (ESSCIRC). ***Thesis topic:*** Low power scalable data converters for edge computing. He is currently with Skyworks, Austin, Tx.

3. **Mohammadhadi Danesh:** Hadi received his PhD in Spring 2020 and authored/co-authored 10 journal and conference publications including first-author publications in IEEE Transactions on Circuits and Systems (TCAS) and IEEE Transactions on Very Large Scale Integration Systems (TVLSI). ***Thesis topic:*** VCO ADC in electrical impedance measurements and Physical Unclonable Function for hardware security application. He is currently with Cirrus Logic, Austin, Tx.

M.S. THESIS STUDENTS GRADUATED

1. **Gokul Ramasamy:** Graduated in Spring 2023 from Arizona State University and co-supervised with Prof. Imon Banerjee. ***Thesis topic:*** Anomaly Detection using Cascade Variational Autoencoder Coupled with Zero Shot Learning – Medical Imaging Use Cases. He is currently a PhD student with Prof. Imon Banerjee at ASU/Mayo Clinic.

2. **Vinay Elkoori Ghantala Karnam:** Graduated in Spring 2021 from State University of New York. ***Thesis topic:*** Hardware implementation of linear SVM classifier for epileptic seizure detection. He co-authored 3 publications during MS in IEEE Solid-State Circuits Letters (SSC-L), IEEE Transactions on Circuits and Systems-I (TCAS-I) and IEEE International Symposium on Circuits and Systems (ISCAS). He is currently with Renesas.

3. **Tushar Gupta**: Graduated in Spring 2021 from State University of New York. ***Thesis topic:*** Hardware implementation of neural network for image classification. He has with Analog Devices after graduation and is a PhD student in my group now.

4. **Naveen Ramesh:** Graduated in Spring 2020 from State University of New York. ***Thesis topic:*** On-chip real-time training of analog artificial neural network classifier circuit for breast cancer classification in 65nm CMOS. He co-authored 2 publications during his MS in IEEE Transactions on Very Large-Scale Integration Systems (T-VLSI) and IEEE International Symposium on Circuits and Systems (ISCAS). He is currently with Qualcomm.

5. **Shivi Chaturvedi:** Graduated in Spring 2019 from State University of New York. ***Thesis topic:*** Design of second order low power delta-sigma modulator using inverter based differential amplifier. She is currently with Qorvo.

6. **Illakiya Venkatesh:** Graduated in Spring 2019 from State University of New York. ***Thesis topic:*** LDPC Code using bit flipping algorithm to increase reliability of a PUF. She co-authored 1 publication during MS in IEEE Transactions on Circuits and Systems -II (TCAS-II). She is currently with Microsoft.

7. **Srinivas Arcot:** Graduated in Spring 2019 from State University of New York. ***Thesis topic:*** Two-stage time-to-digital converter. He co-authored 1 publication during his MS in IEEE Asian Solid-State Circuits Conference (A-SSCC). He is currently with Intel Corporation.

8. **Akshay Jayaraj:** Graduated in Spring 2019 from State University of New York. ***Thesis topic:*** Analog classifier. He taped-out 2 test-chips and authored and co-authored 11 publications during MS including first-author publications in IEEE Asian Solid-State Circuits Conference (A-SSCC), IEEE Transactions on Circuits and Systems- I & II (TCAS-I & II) and IEEE International Symposium on Circuits and Systems (ISCAS). He is currently with Intel Corporation.

9. **Ishita Gupta:** Graduated in Spring 2019 from State University of New York. ***Thesis topic:*** A correlated double sampling assisted capacitance to digital converter. She is currently with Intel Corporation.

10. **Abilash Venkatesh:** Graduated in Spring 2019 from State University of New York. ***Thesis topic:*** 0.3pJ/Bit Machine Learning Resistant Strong PUF Using Subthreshold Voltage Divider Array. He taped-out 1 test-chip and authored 2 first-author publications during his MS in IEEE Transactions on Circuits and Systems-II (TCAS-II) and IEEE International Symposium on Circuits and Systems (ISCAS). He is currently with Intel Corporation.

11. **Nimish Nithin Gujarathi:** Graduated in Spring 2018 from State University of New York. ***Thesis topic:*** Dynamic Comparator Based True Random Number Generator. He co-authored 1 publication during his MS in IEEE Transactions on Circuits and Systems-II (TCAS-II). He is currently with Starkey Hearing Technologies.

12. **Aishwarya Bahudhanam:** Graduated in Spring 2018 from State University of New York. ***Thesis topic:*** Physically Unclonable Functions Based On Voltage Divider Arrays Of MOSFETs Operating In Subthreshold Region. She taped-out 1 test-chip and authored/co-authored 4 publications during her MS in IEEE Transactions on Circuits and Systems-II (TCAS-II), IEEE Transactions on Very Large-Scale Integration Systems (T-VLSI) and IEEE International Midwest Symposium on Circuits and Systems (MWSCAS). She is currently with Intel Corporation.

13. **Archana Ganesh:** Graduated in Fall 2017 from State University of New York. ***Thesis topic:*** Statistical estimator aided SAR ADC design for noise and mismatch suppression. She taped-out 1 test-chip and co-authored 1 publication during her MS in IEEE Transactions on Circuits and Systems-II (TCAS-II). She is currently with Analog Devices.

14. **Saahithi Yammanuru:** Graduated in Spring 2017 from State University of New York. ***Thesis topic:*** Second-order noise shaping time-to-digital converter. She is currently with Cadence Systems.

M.S. PROJECT STUDENTS (CURRENT)

1. **Anoop Bengaluru:** Graduated in Spring 2025 and worked on design of data converters and fabrication of test-chips. Will start as analog design engineer at Cirrus Logic, AZ in summer 2025.

2. **Vincent Chuang:** Graduated in Spring 2025 and worked on design of reference buffers and led the tape-out of a time-to-digital converter test-chip. Will continue as PhD in Fall 2025.

3. **Bhanu Kapa:** Graduated in Spring 2025 and worked on layout design of multiple test-chips. Will continue as assistant research technologist in Summer 2025.

4. **Veeramanikanta Mutyam:** Will graduate in Spring 2026 and is currently designing analog amplifiers and buffers for different test-chips.

UNDERGRADUATE STUDENTS (RESEARCH)

1. **Jiaming Zhang:** He is working on developing a board-level prototype of an AI-based cardiovascular disease classifier.

2. **Jose Sanchez:** Mentored through Fulton Undergraduate Research Initiative (FURI) and currently a PhD student in my group.

3. **Debnath Maiti:** Mentored through FURI and transitioned to MS student in my group.

STUDENTS MENTORED AT OTHER UNIVERSITIES

1. **Shibo Zhou** (PhD student at SUNY Binghampton): Was in Shibo's doctoral committee and co-authored 1 journal and 1 conference paper with him. He is currently with Adaps.

2. **Abraham Peedikayil Kuruvila** (PhD student at UT Dallas): Collaborated on hardware security using machine learning and co-authored 1 journal paper with him. He is currently with Samsung Electronics, Dallas.

3. **Monjoy Saha** (Post-doctoral scholar Emory University): Collaborated on healthcare monitoring using AI and co-authored 2 journal papers and 1 conference paper with him. He is currently a Research Fellow with NIH.

4. **Sanchari Das** (PhD student in SUNY Buffalo): Collaborated on data converter design and testing and co-authored 1 journal paper with her. She is currently continuing her PhD at SUNY Buffalo.

5. **Amartya Bhattacharya** (Undergraduate student in University of Calcutta): Collaborated on AI fusion models during his work at Mayo Clinic and co-authored 1 journal paper with him. He will start PhD at Dartmouth in Fall 2025.

STUDENT FELLOWSHIPS AND AWARDS

1. **Tushar Gupta:** NSF Travel Grant 2025 for attending IEEE MWSCAS.
2. **Sumukh Bhanushali:** University Graduate Fellowship Spring and Fall 2024.
3. **Jose Sanchez:** Fulton Graduate Fellowship
4. **Tushar Gupta:** Fulton Graduate Fellowship
5. **Sumukh Bhanushali:** IEEE Circuits and Systems Society (CASS) Travel Grant, 2024.
6. **Debnath Maiti:** University Graduate Fellowship Fall 2023-Spring 2024.
7. **Vasundhara Damodaran:** ASU Experiential Learning Grant 2023.
8. **Sumukh Bhanushali:** ASU Experiential Learning Grant 2023.

9. **Vasundhara Damodaran:** University at Buffalo Presidential Fellowship Award 2021.
10. **Sanjeev Tannirkulam Chandrasekaran:** Best Paper Award at IBM AI Compute Symposium 2020.
11. **Mohammadhadi Danesh:** Best Paper Award at IEEE MWSCAS Student Design Contest 2019.

COURSES TAUGHT

EEE 527: Analog-to-Digital Converters
This goal of this course to provide a detailed introduction to Nyquist rate CMOS analog-to-digital converters (ADCs). The Nyquist ADC architectures including Flash, Sub-ranging, Pipelined, Folding/Interpolating, Interleaved, and Successive Approximation. Students learn extensive behavioral modeling of ADCs as well as circuit design of complete ADCs using industry standard IC design tool – Cadence.
Semesters taught: Both in-person and online sections in Spring 2025 and Spring 2024.
Weighted average of teaching evaluation score: 4.8

EEE 433/591: Analog Integrated Circuits
The goal of this course is for students to develop the required skills to analyze, design and simulate the core analog circuits such as single stage amplifiers, and operational amplifiers. Biasing, frequency response, design for low power and wide bandwidth, stability, compensation, gain-bandwidth trade-offs are some of the concepts that are used in today's commercial IC design and are covered in this class. The students make extensive use of the professional IC design tool suite – Cadence.
Semesters taught: Online sections in Fall 2024 and Fall 2023, in-person section in Fall 2022.
Weighted average of teaching evaluation score: 3.9

EEE 335: Analog and Digital Circuits
The goal of this course is for students to learn design of both digital and analog circuits, from CMOS logic gates to differential amplifiers, and their simulation using industry standard Cadence EDA tool. The most essential feature of this course is its treatment of the time and frequency domain responses of electronic circuits.
Semesters taught: In-person sections in Spring 2023 and Spring 2022, online section in Fall 2021.
Weighted average of teaching evaluation score: 4.4

EE 491: Analog Circuits (State University of New York)
The goal of this course is for students to learn analysis, design, and simulation of analog integrated circuits. Topics covered: MOSFET small signal model and analysis, single stage amplifier design, frequency response of amplifiers, current mirror, operational amplifier design, gm/Id design methodology, feedback circuit analysis, biasing circuits, and electronic noise.
Semesters taught: Online section in Spring 2021, hybrid section in Spring 2020, in-person sections in Spring 2019 and Spring 2018.
Weighted average of teaching evaluation score: 3.8

EE 559: Digital and Mixed Signal Design (State University of New York)
The goal of this course is for students to learn analysis, design and simulation of mixed signal and digital integrated circuits. Topics covered: sampling theory, sampling circuits, quantizer, electronic noise, switched capacitor circuits, oversampling modulators and combinatorial circuit design.
Semesters taught: Online section in Fall 2020, in-person sections in Fall 2019, Fall 2018, Fall 2017 and Spring 2017.
Weighted average of teaching evaluation score: 4.6

RESEARCH SUPPORT

SUMMARY OF RESEARCH SUPPORT
Dr. Sanyal's share (recognition) in all awards as PI, co-PI, or co-I: $4,972,329*
Total amount of all awards in which Dr. Sanyal is the PI: $3,718,641

*Summation of Dr. Sanyal's share in all current and completed awards listed below

CURRENT AND PRIOR FUNDED PROPOSALS

1. "Radiation Hardened Intelligent Readout ASIC for Nuclear Physics Experiments", Role: PI, Funding Agency: Department of Energy, 04/14/2025-04/13/2027, Amount: $350,000, Dr. Sanyal's share: $350,000, Performance Location: Arizona State University.
2. "C1: Core Project: Machine Learning to RF transceiver Interference Cancelation", Role: Co-PI, Funding Agency: ASU: Connection One Consortium, 9/1/2025-8/31/2026, Amount: $96,405, Dr. Sanyal's share: $60,000, Performance Location: Arizona State University.
3. AWD00040235: "SWAP Project: SMART: Scalable Modular Architecture for RF Transceiver", Role: Co-PI, Funding Agency: Department of Defense, 09/30/2024-09/30/2028, Amount: $10,894,137, Dr. Sanyal's share: $1,400,000, Performance Location: Arizona State University.
4. AWD00040237: "SWAP Project: Spaceborne Low-Energy AI Computing", Role: Co-PI, Funding Agency: Department of Defense, 09/30/2024-09/30/2028, Amount: $32,783,051, Dr. Sanyal's share: $421,904, Performance Location: Arizona State University.
5. AWD00040030: "IDEAS Project: Radiation Hardened Intelligent Readout ASIC for Nuclear Physics Experiments", Role: PI, Funding Agency: NSF IDEAS Center, 08/01/2024-02/29/2028, Amount: $75,000, Dr. Sanyal's share: $75,000, Performance Location: Arizona State University.
6. AWD00039165: "Circuit library for harsh nuclear reactor environment", Role: PI, Funding Agency: DOE, 11/09/2023-08/19/2025, Amount: $60,000, Dr. Sanyal's share: $60,000, Performance Location: Arizona State University.
7. AWD00038721: "Collaborative Research: SCH: Artificial Intelligence Enabled Multi-modal sensor platform for at-home health monitoring of patients with acute kidney injury", Role: PI, Funding Agency: National Institutes of Health, 5/1/2023-4/30/2027, Amount: $1,200,000, Dr. Sanyal's share: $520,803, Performance location: Arizona State University.
8. AWD00039674: "Fast-Response Event-Based Image Sensor and Camera PHASE II", Role: PI, Funding Agency: DOD: Air Force (USAF, 08/07/2023-05/06/2025, Amount: $375,000, Dr. Sanyal's share: $375,000, Performance location: Arizona State University.
9. AWD00039558: "In-Sensor Analog Neural Network Framework for Analog to Information Conversion" Phase-II, Role: PI, Funding Agency: DOE: Advanced Research Projects Agency-Energy (ARPA-E), 8/8/2023-08/30/2025, Amount: $200,000, Dr. Sanyal's share: $200,000, Performance location: Arizona State University.
10. AWD00039575: "On-chip hyperdimensional computing using mixed-signal circuits for Edge AI Semiconductor Research Corporation", Role: PI, Funding Agency: Semiconductor Research Corporation, 06/01/2017-05/31/2020, Amount: $299,998, Dr. Sanyal's share: $299,998, Performance location: Arizona State University.
11. AWD00038409: "Fast-Response Event-Based Image Sensor and Camera", Role: PI, Funding Agency: DOD: Air Force (USAF), 4/10/2023-5/1/2023, Amount: $25,000, Dr. Sanyal's share: $25,000, Performance location: Arizona State University.
12. AWD00038077: "Processing-in-sensor AI circuit for personalized healthcare monitoring", Role: PI, Funding Agency: Sony Corporation, 1/1/2023-12/31/2023, Amount: $100,000, Dr. Sanyal's share: $100,000, Performance location: Arizona State University.
13. AWD00038250: "Large-format CMOS Focal Plane Arrays for Terahertz Imaging Applications", Role: Co-PI, Funding Agency: DOD-DARPA, 12/22/2022-9/21/2024, Amount: $301,979, Dr. Sanyal's share: $45,000, Performance location: Arizona State University.
14. AWD00037778: "Next Generation Cryogenic Electronics for High Energy Physics", Role: PI, Funding Agency: DOE: Advanced Research Projects Agency-Energy (ARPA-E), 8/8/2022-6/26/2023, Amount:

$60,000, Dr. Sanyal's share: $60,000, Performance location: Arizona State University.

15. AWD00037745: "High-Channel Count Electronic Tools for Picosecond (ps) Timing, Role: PI, Funding Agency: DOE: Advanced Research Projects Agency-Energy (ARPA-E), 8/15/2022-6/26/2023, Amount: $60,000, Dr. Sanyal's share: $60,000, Performance location: Arizona State University.
16. AWD00038012: "Fast-framing short-wave infrared (SWIR) cameras for digital-holographic detection", Role: PI, Funding Agency: DOD: Air Force (USAF), 8/5/2022-8/4/2023, Amount: $60,000, Dr. Sanyal's share: $60,000, Performance location: Arizona State University.
17. AWD00037744: "In-Sensor Analog Neural Network Framework for Analog to Information Conversion", Role: PI, Funding Agency: DOE: Advanced Research Projects Agency-Energy (ARPA-E), 8/8/2022-6/26/2023, Amount: $60,000, Dr. Sanyal's share: $60,000, Performance location: Arizona State University.
18. AWD00036891: "FPGA based radiation-hardened camera system", Role: PI, Funding Agency: DOD: Air Force (USAF), 12/1/2021-12/31/2022, Amount: $61,999, Dr. Sanyal's share: $61,999, Performance location: Arizona State University.
19. AWD00037156: "Improved Low Temperature Electronics for Nuclear Physics Experiments", Role: PI, Funding Agency: DOE: Advanced Research Projects Agency-Energy (ARPA-E), 4/6/2022-2/13/2023, Amount: $59,997, Dr. Sanyal's share: $59,997, Performance location: Arizona State University.
20. CISE-1948331: "CRII: SHF: On-chip Multi-Task Learning Analog Artificial Intelligence For Low-Cost Image-Based Environmental Monitoring", Role: PI, Funding Agency: National Science Foundation, 06/01/2020-10/31/2022, Amount: $174,663, Dr. Sanyal's share: $174,663, Performance location: State University of New York.
21. FA8650-18-2-5402: "AI-Flex: An Artificial Neural Network Integrated Flexible Multi-Modal Sensor Patch for Real-Time Continuous Physiological Monitoring and Inference", Role: PI, Funding Agency: Nano-Bio Materials Consortium/Air Force Research Labs (AFRL), 01/01/2020-11/30/2022, Amount: $500,429, Dr. Sanyal's share: $288,314, Performance location: State University of New York.
22. 2712.020: "Low-Power Mostly Digital Time-Domain Delta-Sigma ADCs for IoT", Role: PI, Funding Agency: Semiconductor Research Corporation, 06/01/2017-05/31/2020, Amount: $236,555, Dr. Sanyal's share: $236,555, Performance location: State University of New York.

PROFESSIONAL ACTIVITIES AND SERVICE

SUMMARY OF PROFESSIONAL ACTIVITIES AND SERVICE
Editor, Associate Editor for 4 peer-reviewed journals
3 International/national conferences chaired
8 International/national conferences committees
Member of Editorial Board 4
Peer Reviewer for 7 Journals
Proposal Review Service for Funding Agencies 8
Engineering School-level Committees 2

SELECTED SERVICE

1. ***Associate Editor:*** IET Electronics Letters, Frontiers in Electronics, Scientific Reports, Guest Editor for Elsevier Memories: Materials, Devices, Circuits and Systems.

2. ***Member of Technical Program Committee:*** Analog Signal Processing Technical Committee (ASP-TC) of IEEE Circuits and Systems society, VLSI Systems and Applications Technical Committee (VSA-TC) of IEEE Circuits and Systems society, IEEE Radio and Wireless Week (RWW), IEEE VLSI Design and Embedded Systems (VLSI-D), IEEE/ACM Design Automation Conference (DAC), IEEE VLSI Test Symposium (VTS), IEEE Midwest Symposium on Circuits and Systems (MWSCAS), Custom Integrated Circuits Conference (CICC).

3. ***Sessions/Track Chair:*** 2026 IEEE VLSI Test Symposium publication chair, 2025 IEEE VLSI Test Symposium publicity chair, 2023 IEEE VLSI-D Analog and Mixed Signal track chair, 2022-2024 IEEE RWW high-speed data converters track chair, 2023 MWSCAS sponsorship co-chair, 2020 IEEE MWSCAS Analog Circuits and Systems session chair.

4. ***Referee:*** IEEE Journal of Solid-State Circuits, IEEE Transactions on Circuits and Systems (I & II), IEEE Transactions on Very Large Scale Integration Systems, IEEE Transactions on Biomedical Circuits and Systems, IEEE Transactions on Biomedical Engineering, IEEE Open Journal of Circuits and Systems.

5. ***Proposal review service:*** Reviewer for NSF ASCENT panel, NSF CISE panel, NSF GRFP panel, DoE Office of Science, NIH CSR Panel, NIH Special Emphasis Panel for Small Business, American Heart Association (AHA), Swiss National Science Foundation.

6. ***Engineering School-level Committees:*** Member of ASU New Faculty Advisory Council (NFAC), ASU's Quality of Instruction Committee

7. Technical working groups: Member of Semiconductor Research Corporation's Microelectronic and Advanced Packaging Technologies Roadmap (MAPT 2.0) for Analog/Mixed Signal group and Security and Privacy group.