MANI JANAKIRAM, PhD **Phone: (480) 203-7259**
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SUMMARY

Proven leader with expertise in supply chain, manufacturing, automation, quality, people management, project management, teaching, research, strategy, operational & cost modeling, cycle time reduction, benchmarking, and problem solving. Successfully combines domain knowledge with analytics and people skills to deliver key solutions that enables innovation, efficiency & effectiveness.

EXPERIENCE

Intel Corporation, Chandler, Arizona 1999 - Current

Director, Supply Chain Strategy & Analytics

Managed Intel's supply chain strategy, SCOR, benchmarking, SC innovation, modeling and analytics, Supply Chain Master/Technologist program, university relations, external engagements, SC research, Recent College Graduate program and developing path-finding solutions for supply chain across Intel.

Accomplishments

- Managed the SC strategy and roadmap to ensure SC industry leadership and successfully implemented new SC capabilities. Identified key supply chain needs for the next 3+ years and delivered a roadmap to generate millions of dollars of business value.
- Manage a team of 40+ supply chain professionals and managers to provide flawless supply chain service across Intel.
- Managed SNSC, Biz summit, CPLG SOs/IMBOs. Implemented RCG program and collaborative SC benchmarking system.
- Developed scenario analysis and decision metrics for capital equipment, sourcing, product ramp and inventory mgmt. to enable optimal supply-demand solutions.
- Developed various BI solutions to ensure high quality decision making in supply chain planning, network and transportation. Developed analytical framework (optimization, statistics, DM, simulation) to solve complex supply chain challenges.
- Established simulation & analytics roadmap to address key SC challenges. Delivered effective analytical solutions across Intel's supply chain that has saved >$100M.
- Established RCG hiring/sourcing/training strategy for Intel in Asia and USA resulting in a healthy hiring pipeline.
- Developed demand forecasting, SC cost and inventory planning algorithms to improve forecast accuracy and reduce inventory.
- Co-chair of HVMRC (>$1M budget) and managing Intel's six Supply Chain Research programs to solve critical challenges. Implemented several research projects leading to innovative solutions with millions of dollar savings.
- As a Lean Six Sigma Master Blackbelt, developed Forecasting techniques for supply chain, developed forecasting and analytical modules and taught several courses on lean six sigma. Mentored several lean sigma candidates successfully.
- Delivered several keynotes on supply chain at leading supply chain conferences/workshops to improve Intel's supply chain branding
- Developed TMG finance revenue forecasting models to reduce forecasting variability by >20%. Received **Intel Trade Secrete.**
- As a Principal Engineer, provided statistical guidance to the development of FCC guidelines on Broadband. Received **DRA.**

Staff Manager TME (ODST & ACT) and LTDA (previous positions within Intel)

Responsible for process control development & deployment, mfg systems, research, data integration, department mgmt, development of analytics & visualization tools and technical leadership in data mining, process control, modeling and factory operations.

Accomplishments

- Led the consolidated PCS effort (FSM, LTD, ATM) to deliver a converged Off-line PCS roadmap for TMG. The converged Off-line PCS strategy was one of the highlights demonstrating the value achieved with the SET efforts to the TMG Automation.
- Successfully managed a group of 60+ ACT engineers with significant accomplishments. Led product development & support strategy, roadmap development, customer service strategy, solution integration, resource planning and performance metrics.
- Served as global/US ITRS factory integration chair and developed short-term/long-term factory integration strategy, technical requirements and potential solutions. Benchmarked operations metrics to compare against Intel metrics.
- Led Intel's 1st FSM capital capacity systems to establish data driven decision tools/systems (over $100M savings, 4+ days improvements in planning TPT). Managed 100+ people with a $5M budget. Received **Intel Achievement Award** and **DRA's**.
- Managed/developed several analytics projects/solutions involving lean, simulation, optimization, process reengineering projects for cycle time improvement, cost reduction and productivity improvement. Led **TME's IQA** quality sub-team successfully.
- Chaired factory operations research center ($1M/yr for 6 yrs - 50 students, 10 universities & 12 company consortia), completed 12+ projects in factory operations, APC, PM. Received "**Mentor of the year**" award from Semiconductor Research Organization.
- Managed Intel's 1st 200mm APC program and successfully implemented SRC/EFCC litho APC (> 20% improvements). Developed litho APC non-linear, multivariate algorithm for registration and CD feedback control. Received **Excellence Award**.
- Developed several stochastic solutions (AMHS, Equipment, and Supply chain) that complemented simulation techniques to provide quick and accurate prediction techniques. Received **Intel Trade Secrete**.

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Motorola, ACT, Semiconductor Products Sector, Mesa, Arizona 1995 - 1999
Manager / Principal Staff Engineer, Manufacturing Systems & Planning
Responsible for planning, manufacturing engineering, systems and support of fab modeling, automation, cycle time reduction, production control, project management, manufacturing database, benchmarking, materials management and capacity planning.

Accomplishments
- Managed ACT's planning group to drive supply-demand alignment with business units, capacity planning, production control, incoming materials mgmt, inventory control, RMA, shipping and integration of supply chain planning tools (i2, PROMIS, SAP).
- Developed, analyzed and managed various fab reports and ACT's manufacturing database. Developed database to manage ACT wafer usage and wafer inventory. Delivered >**40% cost savings** in wafer inventory. Received Six Sigma Black Belt certification.
- Developed roadmap for transitioning ACT from a development fab to a manufacturing & development fab. Performed extensive Simulation & optimization and played a key role in MOS production ramp-up (**over $10 million impact**).
- Successfully developed ACT fab model to perform capacity planning, identify fab bottlenecks, optimized WIP, maximize throughput and perform "what-if" analysis. Implemented real-time WIP & equipment monitoring systems (improved WIP by 10%).
- Led cycle time reduction effort to improve cycle time, equipment usage, WIP and throughput. The 35% improvement in cycle time received **highest SPS recognition**. Benchmarked fab performance metrics to improve Motorola fab metrics.

Special Devices, Inc., Automotive Division, Mesa, Arizona 1992 - 1995
Senior Manufacturing Engineer
Responsible for manufacturing management & support, assembly/test equipment sourcing, automation, benchmarking, cost-benefit analysis, project management and total quality management.

Accomplishments
- Supervised 3 automation teams comprising of engineers, technicians and operators. Performed enterprise analysis using CIM tools to analyze bottlenecks in manufacturing processes. Developed automation solutions for assembly & testing of airbag initiators.
- Chaired scrap reduction committee on welding processes and was instrumental in reducing the scrap rate by 8% and reducing downtime by 20% resulting in a **saving of $200K per year**.
- Performed capacity planning, DOE, cost modeling, simulation, Lean, and statistical analysis to optimize process flow and layout.
- Served as project leader with ASU to develop bar code to support SDI's manufacturing execution system.
- Streamlined operating procedures & process mapping for various processes and trained technicians and operators.
- Developed techniques to reduce scrap and increase productivity in lapping and cleaning of parts resulting in **~$90K savings/year**.

Allied Signal Aerospace Company, (Honeywell), Phoenix, Arizona 1990 - 1992
Manufacturing Science Engineer
Responsible for project management, machinability evaluation, process simplification, data analysis, technology evaluation and implementation. Major emphasis was on technology development, process cost & scrap reduction.

Accomplishments
- Developed machining and cleaning techniques for Titanium Metal Matrix Composites (**two patents received**).
- Wrote proposal for developing and demonstrating an improved manufacturing process for U720 disk slot machining. Secured the army contract for implementing project. Served as Project Leader and led a team of engineers, operators, consultants and suppliers. Optimizing the broaching parameters resulted in **34% reduction** in cycle time and **25% reduction** in tool cost.
- Performed economic & statistical analysis, simulation and cost benefit analysis on various manufacturing processes.

Widia (India) Limited, (Kennametal, USA), Bangalore, India 1984 - 1988
Project/Assembly Engineer
Responsible for planning, design, supplier coordination, assembly, testing, and customer support of special purpose machines.

Accomplishments
- Led a team of technicians in developing several special purpose machines. Key member of the team that designed and built IMTEX award winning CNC universal gun drilling machine.
- Performed plant layout, economic analysis, capacity planning, equipment specification & purchase for a new mfg. department.
- Developed several fixtures & optimized gun drilling parameters for mining tools that resulted in over **30% savings** in scrap.

EDUCATION

MBA in International Management, Thunderbird School of Global Management, AZ 2006
Ph. D. Industrial & Management Systems Engineering, Arizona State University, AZ 2001
M. S. Industrial & Management Systems Engineering, Arizona State University, AZ 1990
B. S. Mechanical Engineering, University of Mysore, India 1984

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AWARDS & AFFILIATIONS

- APICS **Certified Supply Chain Professional** (**CSCP**)
- Intel certified **Lean Six Sigma Master Black Belt** and Motorola certified **Six Sigma Black Belt**
- Completed Project Mgmt, Leadership training, APICS training, Lean and Theory of Constraints training.
- One of the 81 engineers selected by **National Academy of Engineering** for 2006 Frontiers of Engineering Symposium.
- Honorary MIT Scale **Visiting Lecturer**, MIT, Cambridge, MA
- **Adjunct Faculty** at Arizona State University School of Business, Tempe, AZ
- **Adjunct Faculty** at Thunderbird School of Global Management, Glendale, AZ.
- Received "**Intel Achievement Award**", the highest honor at Intel for outstanding achievement.
- Received 2 **US Patents** (#5415336, #5373983) for composite machining and bonding techniques.
- Semiconductor Research Corporation – **Mahboob Khan Mentor Award** (1999 & 2003), Leadership recognitions.
- Received "**Brumbaugh Award**" from American Society of Quality for best journal paper & contribution to quality.
- ASQ **Certified Quality Engineer** from ASQ and **Certified Manufacturing Engineer** from SME.
- Serves/d on several research committees including, Sematech Industry Economic Modeling, Stanford AIM, ASU Supply Chain Board, MIT Center for Transportation & Logistics.
- Serving as judge on the Arizona Governor's Celebration of Innovation Nomination Committee.
- Regularly gets invited by universities, consortia and organizations to deliver presentations on supply chain, lean six sigma, factory operations, analytics and strategy.
- Served on NSF proposal selection panels and as chaired several conference tracks (INFORMS, WinterSim and others).
- Published 75+ papers (Journals, Conference Proceedings, Invited Speaker, etc. (*list available upon request*).

Mani Janakiram Publications & Presentations - 1995 to Current only

1. Amit Shinde, Moeed Haghnevis, Marco Janssen, George Runger, Mani Janakiram, “SCENARIO ANALYSIS OF TECHNOLOGY PRODUCTS WITH AN AGENT-BASED SIMULATION AND DATA MINING FRAMEWORK”, International Journal of Innovation and Technology Management, Vol. 10, No. 5 (2013)
2. Mani Janakiram, “Enabling Intel’s Supply Chain through Effective Analytics”, Invited Speaker, Big Data in the Supply Chain Conference, June 2013
3. Mani Janakiram, “SC Evolves to Enable Industry Evolution”, Invited Speaker, MIT CTL Crossroads 2013: Supply Chain as Future Enabler, June 2013
4. P. Pekgün, P. Keskinocak, M. Janakiram, T. Maku “Investigating Strategic Customer Behavior through Interactive Supply Chain Game”, Behavioral Operations Management Conference, Washington, June 2012
5. Mani Janakiram, “Enabling Intel’s Supply Chain through Effective Analytics”, Invited Speaker, INFORMS Conference on Business Analytics and Operations Research, April 2012
6. Mani Janakiram, “Intel Supply Chain Challenges”, **Invited Speaker**, 5th Annual Hi-Tech & Electronics Supply Chain Summit - The Americas, November 2011
7. Pinar Keskinocak, Shuangjun Xia, Mani Janakiram and Tosanwunmi Maku, “Supply Chain Game”, OR/MS Today, October, 2011
8. Amit Shinde, George Church, Mani Janakiram, George C. Runger: Feature extraction and classification models for high-dimensional profile data. Quality and Reliability Eng. Int. 27(7): 885-893, 2011
9. Pinar Keskinocak, Mani Janakiram, Tosan Maku, “A New Supply Chain Game: Assess Supply Chain Strategies with Interactive Simulation”, submitted to Analytics Magazine, November 2011
10. Ana Cristina Barros, Edgar Blanco, Ana Barbosa-Povoa, Mani Janakiram, “The Seven Deadly Supply Chain Phenomena”, submitted to International Journal of Logistics Management, October 2011
11. Pinar Keskinocak, Mani Janakiram, Tosan Maku, Supply Chain Game, Informs Online, October 2011
12. Fang Li, George Church, Mani Janakiram, Howard Gholston, George C. Runger: Fault detection for batch monitoring and discrete wavelet transforms. Quality and Reliability Eng. Int. 27(8): 999-1008, 2011
13. Mani Janakiram, Supply Chain as a Key Driver at Intel, Supply Chain Brain, August, 2011
14. Cindie Blackmer, Mani Janakiram, “Breaking Down Supply Chain Silos through Strategy to Action” SC Innovation Award Finalist Presentation, CSCMP Annual Global Conference, 2010
15. M. Janakiram, H. Shah, “Integration of Lean and Six Sigma for maximizing benefits”, **Invited speaker**, ASQ 2010 Lean and Six Sigma Conference, April 2010
16. M. Janakiram,”Supply Chain Planning and Analytics at Intel”, **Invited speaker**, Operarional Research and Industrial Engineering Seminar, University of Texas, Austin, September 2009
17. A. Alan, M. Janakiram, et al “ITRS 2007 Highlights for Semiconductor International Webcast”, Panel Discussion, Jan 2008
18. M. Janakiram, “Lean Six Sigma for Business Improvement”, **Invited speaker**, Knowedge Sharing and Conuslting Club, Thunderbird School of Global Management, June 2008
19. R. Das, G. Runger G. Church, M. Janakiram, “Wavelets for Dynamic Time Warping Distance”, submitted to IEEE Transactions on Semiconductor Manufacturing, April 2008
20. N. Govind, E. Del Castillo, G. Runger, M. Janakiram, “An Approach to Multivariate Process Adjustment”, submitted to Journal of the Operational Research Society (JORS), Dec 2008
21. M. Janakiram, “ITRS Factory Integration Perspecitve on Next Generation Factory Challenges and Needs”, **Invited speaker**, SEMI Technology Symposium, Semicon Japan 2007, Makuhari Messe, Japan, Dec 2007
22. M. Janakiram, “2007 ITRS Factory Integration Update”, ITRS/IRC Press, Makuhari Messe, Japan, Dec 2007
23. O. Arda Vanli, Nital S. Patel, Mani Janakiram, Enrique Del Castillo, “Model Context Selection for Run-to-Run Control”, IEEE Transactions on Semiconductor Manufacturing, Vol. 20, Issue 4, Nov 2007
24. M. Janakiram, “ITRS Factory Integration perspective on AEC/APC”, **Invited speaker**, 8th European Advanced Equipment Control/Advanced Process Control (AEC/APC) Conference, Dresden, Germany, April 2007
25. O. Arda Vanli, Nital S. Patel, Mani Janakiram, “A flexible methodology and simulation capability for APC (Advanced Process Control) algorithm development and validation in semiconductor manufacturing processes” submitted to IEEE TSM, Oct 2006
26. M. Janakiram, “2006 ITRS Factory Integration Update”, ITRS/IRC Press, Hsinchu, Taiwan, Dec 2006

27. Mani Janakiram, “Factory Operations Research Center (FORCe) addressing the Semiconductor Industry short term and long term research needs” submitted to IEEE T-ASE, Nov 2006
28. José A. Ramírez-Hernández, Jason Crabtree, Xiaodong Yao, Emmanuel Fernandez, Michael C. Fu, Mani Janakiram, Steven I. Marcus, Matilda O’Connor, and Nipa Patel, “Optimal Preventive Maintenance Scheduling in Semiconductor Manufacturing Systems: Software Tool & Simulation Case Studies”, submitted to IEEE TSM, July 2006
29. M. Janakiram, “ITRS Factory Integration Update”, ITRS/IRC Press, San Francisco, July 2006.
30. M. Janakiram “Semiconductor Factory Integration Challenges & Research Needs”, Invited speaker, Dept. of Industrial Eng. – **Invited speaker**, Lehigh University, June 2006.
31. M. Janakiram “Semiconductor Factory Integration Challenges & Research Needs”, Invited speaker, Dept. of Industrial & Systems Eng. – **Invited speaker**, University of Texas, Austin, July 2006.
32. P. Backus, M. Janakiram, S. Mowzoon, G. Runger, and A. Bhargava, “Factory Cycle-Time Prediction with a Data-Mining Approach”, IEEE Transactions on Semiconductor Manufacturing, Vol. 19, Issue 2, May 2006.
33. M. Janakiram, “Factory Integration Overview", **Invited speaker**, 17th Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC 2006), May 2006.
34. M. Janakiram, “Factory Integration”, The Hot Button, Micro Magazine, April 2006.
35. M. Janakiram, “ITRS Factory Integration Webcast", **Invited speaker**, 2nd Annual Electronics Manufacturing Summit, Semiconductor International, April 2006.
36. M. Janakiram, Lance Solomon “Factory Integration Challenges and Application of Industrial Engineering Concepts within Intel”, **Invited speaker**, Sichuan University, Chengdu, China, March 2006.
37. M. Janakiram, “ITRS Factory Integration and Facilities Cross-Cut Issues", **Invited speaker**, Arizona State University, CREATE, Phoenix, AZ, March 2006.
38. M. Janakiram, “Factory Integration Roadmap", **Invited speaker**, ISMI Global Economic Symposium, ISMI 2006 Symposium, San Jose, CA, Jan 2006
39. M. Janakiram, “Factory Integration Challenges & Research Needs”, M. Janakiram, **Invited speaker**, Dept of Industrial Engineering, National Taiwan University, Taipei, Taiwan, Dec 2005
40. M. Janakiram, “ITRS Factory Integration and FORCe Overview ", presented to TSMC Senior Management, Hsinchu, Taiwan, Dec 2005
41. M. Janakiram, “ITRS FI 2005 Presentation”, ITRS/IRC Press, Seoul, South Korea, Dec 2005
42. M. Janakiram, “Lean Six Sigma for Process Improvement”, **Invited speaker**, NIQR, Bangalore, India, Dec 2005
43. M. Janakiram, S. Goernitz, “Real Time Lithography Registration, Exposure and Focus Control – A Framework for success”, IEEE Transactions on Semiconductor Manufacturing, Nov 2005
44. M. Janakiram, “What Managers Seek in Graduates”, **Invited speaker**, Informs Colloquium, San Francisco, CA, Nov 2005
45. M. Janakiram, “ITRS Factory Integration Overview ", **Keynote speaker**, ISMI 2005 Symposium on manufacturing Effectiveness, Austin, TX, Oct 2005
46. M. Janakiram, “Semiconductor Factory Integration Challenges & Research Needs”, **Invited speaker**, Dept of Mechanical Engineering – Oct’05 Manufacturing Seminar, University of Michigan, Ann Arbor, MI, Oct 2005
47. M. Janakiram, “University / Industry Engagements for Process Control”, **Invited speaker**, Intel APC summit, Sep 2005
48. M. Janakiram, “ITRS Factory Integration 2005 Update”, ITRS Press, San Francisco, July 2005
49. M. Janakiram and G. Runger, “Fundamentals of Data Mining and Applications to Factory Data”, **Invited speaker**, INFORMS, April 2005
50. M. Janakiram, “Role of Statistical Modeling & Analysis in Semiconductor Manufacturing Research”, **Invited speaker**, Intel Stat Summit, April 2005
51. A. Greenburg, M. Janakiram, S. Kobayashi, T. Chen, “ITRS Factory Integration Update”, SEMICON Europe, April 2005
52. J. Pettinato, M. Janakiram, “An ITRS Perspective On 300 mm Factory Advances And A Vision For Future Breakthrough Enterprise Performance”, Future Fab Intl. Volume 18, January 2005
53. N. Govind, M. Janakiram, Russell R. Barton and G. Runger. “Multivariate Control of a Semiconductor Manufacturing Process”, WinterSim, 2004
54. M. Janakiram and S. Goernitz, “Real Time Lithography Registration, Exposure and Focus Control – A Framework for success”, IMEC 2004

55. P. Tung, M. Janakiram, S. Wu, “Constraint tool run rate improvement – using tool-level simulation combined with response surface modeling on Smema Chip Attach Module (SCAM)”, IMEC 2004
56. M. Janakiram, S. Movafagh, “Fab TPT prediction using data mining techniques”, IMEC 2004
57. M. Janakiram and S. Goernitz, “Real Time Lithography Registration, Exposure and Focus Control – A Framework for success”, ISSM 2004, Tokyo, Japan (selected as one of the **Best papers** to be published in IEEE Transactions for Semiconductors)
58. R. Goodwin, R. Miller, E. Tuv, A. Borisov, M. Janakiram, S. Lochheim, “Advancements and Applications of Statistical Learning/Data Mining in Semiconductor Manufacturing”, Intel Technology Journal, Nov 2004
59. A. Greenburg, M. Janakiram, S. Kobayashi, T. Chen, “ITRS Factory Integration Update, ITRS press/SEMICON, Taiwan Dec 2004
60. M. Janakiram, J. Fowler, F. Robertson and K.J. Stanley, “Overview of the Factory Operations Research Center”, INFORMS Conference, 2003
61. M. Janakiram, J. Fowler, F. Robertson and K.J. Stanley, “Impact of Factory Operations Research (FORCe) on Semiconductor manufacturing”, INFORMS Conference, 2003
62. N. Govind, E. Del Castillo, G. Runger and M. Janakiram, “Multivariate Bounded Adjustment Policies”, INFORMS Conference, 2003
63. P. Backus, M. Janakiram, G. Runger and S. Movafagh, “Lot cycle time prediction using data mining”, INFORMS Conference, 2003
64. C. Maloney, V. Pagano, M. Janakiram, “Lithography Process Control at Intel”, AEC/APC Conference, 2003
65. T. Roeder, S. Fischbein, M. Janakiram, and L. Schruben, “Resource-Driven and Job-Driven Simulations”, Proceedings of the 2002 International Conference on Modeling and Analysis of Semiconductor Manufacturing: 78-83, 2002
66. M. Janakiram, D. Montgomery, B. Keats, “Integration of EPC and SPC for effective Process Control”, ASQ Fall Tech Conference, 2002
67. M. Janakiram, D. Montgomery, B. Keats, “Integrating EPC and SPC for effective APC”, QPRC, 2002
68. M. Janakiram, “FORCe - A Collaborative Factory Operations Research for Manufacturing Excellence”, Semiconductor Research Corporation publication, 2002
69. M. Janakiram, J. Fowler, F. Robertson and K.J. Stanley, “A Factory Operations Research for Semiconductor Manufacturing Excellence”, INFORMS Conference, 2002
70. Mani Janakiram, Statistical and engineering process control integration strategies for constrained controllers, PhD Thesis, Arizona State University, 2001
71. M. Janakiram, D. Pillai, “Operational Modeling at Intel”, MASM Conference, 2000
72. M. Janakiram, S. Nugent, “Capacity planning and modeling at Motorola’s ACT Fab”, HP Web hosted seminar, 1999
73. J. Morrison, M. Janakiram, P.R. Kumar, “Evaluation of scheduling policies in the semiconductor fab”, MASM Conference, 1999
74. J. Morrison, M. Janakiram, P.R. Kumar, “A comparative study of scheduling policies at Motorola fabs”, Proceedings of the 1999 SMOMS Conference, San Jose, CA, 1999
75. M. Janakiram, J. Morrison, “Capacity planning and study of scheduling policies using simulation at Motorola's ACT fab,” Proceedings of the 1999 SMOMS Conference, San Jose, CA, 1999
76. M. Janakiram, “A tutorial on Theory of Constraint application to ACT fab”, Motorola TEM, 1999
77. P. Ocansey, M. Janakiram, “Impact of Megasonics on the bath life of SC-1 Cleaning” Micro, June 1998
78. M. Janakiram, “Capacity Modeling at Motorola’s ACT Fab”, Tyecin Advanced Planning, Scheduling and Analysis Conference, Palo Alto, CA, May 1998
79. M. Janakiram, B. Keats, “Combining SPC and EPC in a Hybrid Industry”, Journal of Quality Technology, Vol 30, No. 3 P189-308, 1998 (Received prestigious “**Brumbaugh Award” from American Society of Quality for best journal paper** which has made the great contribution to the development of industrial applications of quality control in 1998)
80. M. Janakiram, “Integration of SPC and EPC for Process Improvement” Six Sigma Black Belt Symposium, 1997
81. M. Janakiram, D. Cambron, “Real-time lot monitoring and cycle time analysis at ACT”, Motorola TEM, 1997
82. M. Janakiram, “OEE at Motorla’s ACT Fab”, Sematech Workshop, Phoenix, AZ, 1997
83. M. Janakiram, “Cycle Time Reduction at Motorola’s ACT Fab”, ASMC ’96 Conference, Boston, MA, 1996

84. Ren, J.J., M. Liaw, B. Turner, C. Stein, F. Hampton, T. Merchant, and M. Janakiram, “Rapid thermal oxidation on Si/SiGe strained layer heterostructures”, Proc. 4th Intl. Conf. on Advanced Thermal Processing of Semiconductors, (RTP'96), 1996
85. M. Janakiram, B. Keats, “Application of FMEA in Process Quality Improvement", International Journal of Reliability, Quality and Safety Engineering, Vol 2, No. 1 P103-105, World Scientific Publishing Company, 1995
86. U.S. Patent Number 5,415,336: Method for preparing a composite surface for diffusion bonding, Steven Stenard, Mohsen Sohi, Donald Schuyler, Mani Janakiram, May 1995.
87. U.S. Patent Number 5,373,983: Composite article having a surface prepared for diffusion bonding, Steven Stenard, Mohsen Sohi, Donald Schuyler, Mani Janakiram, December, 1994
88. Mani Janakiram, Study of metal cutting chip formation using statistical techniques, MS Thesis, Arizona State University, 1990
89. Published 10+ papers before 1995