

TUSHAR GUPTA

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EDUCATION

Arizona State University, AZ - Ph.D. in Electrical Engineering

August 2023 - Present

University at Buffalo, NY - MS in Electrical Engineering

August 2018 - July 2020

Relevant Courses: RF Circuits, Analog Circuits, Mixed Signal, MIMO, Digital Communication, Device Physics, Machine Learning

Jaypee Institute of Information Technology - B.Tech in Electronics and Communication Engineering

July 2010 - May 2014

TECHNICAL SKILLS

Analog Circuit Design: Opamps, Filters, Amplifiers, Bias, Feedback, Compensation, LDO, Comparators, Switched Capacitors

EDA Tools: Cadence Virtuoso, Keysight ADS, Quartus Prime Lite, SPICE, Eagle PCB CAD, LabView, TestStand

Lab Equipment: Oscilloscope, Signal Generator, Vector Network Analyzer, Spectrum Analyzer, Logic Analyzer, ATE, NI DAQ

Programming: MATLAB, C, Python

PROFESSIONAL EXPERIENCE

Qorvo Inc., Senior Test Engineer, Greensboro, NC

January 2023 - June 2023

- Developed production test solutions for Automotive products using ATE hardware and software systems
- Coordinated with test, design, and product engineering to develop production test plans for RF front-end modules

Analog Devices Inc., Product Engineer, Norwood, MA

March 2021 - January 2023

- Tested transceiver chip for drift in signal power due to temperature
- Worked with design, software, and application teams to resolve a bug that degraded the transceiver's LO leakage
- Evaluated the multi-carrier 5G use case for the transceiver by checking the ACLR performance across channels
- Ran regressions over Software Verification bench to evaluate the performance of the transceiver across releases

Esensors Inc., Electronics Research Engineer, Amherst, NY

July 2020 - March 2021

- Developed an acoustic telemetry system using Frequency Shift Keying (FSK) at 10 kHz for monitoring CO₂
- Amplified, regulated, and filtered noise in the receiver signal using OPAMP, LDO, and Butterworth filter
- Designed and developed a wireless communication system to detect hydrogen using NFC, ZigBee, and PIC
- Created wireless pore water sensor to measure underground pressure, temperature, and moisture using PIC

Infosys Ltd, Senior Systems Engineer, Bangalore, India

June 2014 - March 2017

- Implemented update manager for Microsoft Windows, CentOS
- Developed python script to track system performance in Linux environment to increase stability by 15%

Prasar Bharti, Summer Intern, Delhi, India

June 2013 - July 2013

- Worked with RF transceivers and dish antennas to understand broadcasting and signal reception from satellite
- Learned about Direct-to-Home (DTH) service and its internal components

RESEARCH EXPERIENCE

Arizona State University, AZ- Graduate Research Associate, Analog/Mixed Signal Lab

August 2023 - Present

- Assisted custom tape-out of Reservoir Computing and Neural Network chip utilizing 9T1C SRAM Cell (TSMC-28)
- Automated hardware test setup for the Reservoir Computing based AI to predict Earthquake and Human Activity Recognition
- Developed MATLAB model for Hyper-Dimensional Computing (HDC) AI to classify heart sounds from phonocardiogram
- Developing a mixed signal-based integrator circuit utilizing dynamic amplifier and bottom-plate sampling switch for HDC

University at Buffalo, NY - Graduate Researcher, Analog/Mixed Signal Lab

August 2019 - July 2020

- Designed switched Capacitor based Neural Network for Image Classification (TSMC-65)
- Prototype achieves 88% accuracy with the efficiency of 10.1 nJ/classification
- Programmed Pulse Function Arbitrary Noise Generator using MATLAB to generate periodic/aperiodic signals
- Programmed Mixed Signal Oscilloscope using MATLAB to capture data from analog and digital waveforms

ACADEMIC PROJECTS

Telescopic Cascode differential Amplifier design in Cadence Virtuoso (TSMC-250)

- Designed a telescopic cascode amplifier using beta multiplier based current reference
- Achieved a gain of 60.5 dB, phase margin of 67.3 degrees and unity gain frequency of 51.2 MHz

Bootstrapped NMOS Sampling Switch design in Cadence Virtuoso (TSMC-180)

- Designed a bootstrapped NMOS sampling switch for 51 MHz sampling frequency and 4.7 MHz input frequency
- Utilized bottom-plate and differential sampling to achieve 70 dB SNDR along with high linearity

Low Dropout Regulator Design in Cadence Virtuoso (TSMC-250)

- Designed a PMOS LDO for an input supply of 3V to get output voltage of 2.8V with peak PSRR of 54.898 mDB
- Achieved phase margin of 60 degrees. Got overshoot voltage of 156.37 mV and undershoot of 106mV for 0-50mA current rise

Two Stage Opamp design in Cadence Virtuoso (TSMC-250)

- Developed a 2-stage opamp using Miller compensation
- Utilized gm/id technique and achieved a gain of 72 dB and a phase margin of 60.3 degrees

Switched Capacitor amplifier design in Cadence Virtuoso (TSMC-180)

- Developed a switched capacitor amplifier with precision gain of 4 using 2-stage Miller OTA and bootstrap switch
- Incorporated gm/id technique to achieve 72.4 dB gain and 0.08% static settling error

Active RC Low-Pass Filter design in Cadence Virtuoso (TSMC-180)

- Developed filter using miller compensation technique to attain 1.0375MHz bandwidth
- Utilized gm/id technique to design OTA and achieved a gain of 72.4 dB

PUBLICATIONS:

- Tushar Gupta, Vasundhara Damodaran, Jose Sanchez, and Arindam Sanyal, "Heart Abnormality Detection from Phonocardiogram Signals Using Reservoir Computing", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2025.
- Tushar Gupta, Vasundhara Damodaran, and Arindam Sanyal, "Reservoir Computing based AI for Estimating Remaining Useful Life of Turbofan Engine", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2025.
- Vasundhara Damodaran, Jose Sanchez, Tushar Gupta, Phaneendra Bikkina, Esko Mikkola, Abdul-Muhsin Haidar, Imon Banerjee, and Arindam Sanyal, "AI-Enabled Fusion of Electrocardiograph and Demographics for Prediction of Acute Kidney Injury Onset", *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2024.
- Sumukh Bhanushali, Tushar Gupta, Debnath Maiti, and Arindam Sanyal, "Machine Learning Based Static and Dynamic Error Calibration in Data Converters", *IEEE VLSI Test Symposium (VTS)*, (invited paper), 2024.

PATENTS AND AWARDS:

- Provisional Patent Application No. 63/553,345 - "Machine Learning Enhanced Analog-to-Digital Converters"
- Fulton Fellowship (Fall '23-Spring' 24, Fall' 24-Spring' 25, Fall'25-Spring'26)
- MWSCAS 2025 NSF Student Travel Grant