SOUMYOJIT NAG

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Summary

Results-driven professional with 3 years of experience as a Mixed-Signal LSI Characterization and Validation Engineer. Expertise in bench testing, post-silicon IC validation, and project management. Seeking an Analog and Mixed Signal Design Intern role.

Education

Arizona State University (Tempe, AZ, USA) August 2024 - Present
MSE in Electrical Engineering - Analog and Mixed Signal IC Design 3.85 / 4 CGPA
Relevant Courses: Advanced Analog Integrated Circuit Design; Analog Integrated Circuit Design; Digital System & Circuit.

SRM University (Chennai, TN, India) July 2017 – June 2021
Bachelor of Technology in Electrical & Electronics Engineering 8.52 / 10 CGPA

Skills Summary

- Design and execute comprehensive post-silicon validation plans
- Identify and troubleshoot IC issues through detailed testing debug processes.
- Proficient with bench lab instruments such as oscilloscope, source meter, thermo stream, thermal chamber, frequency analyzer, AC-DC power supply, Arbitrary Function Generator.
- Tools & Technologies: Cadence –Virtuoso, Kickstart, Eagle CAD, Altium PCB Design, LT Spice, MultiSIM.

Academic Projects

Design and Analysis of a Telescopic Cascode Differential Amplifier stage:

- Specifications: Supply voltage of 3.0-3.5V supply, DC gain>50dB, wide bandwidth, and robust biasing for differential signal processing applications.
- Design Features: Achieved 50dB+ DC gain, 50MHz unity gain frequency with a 1pF load, and 1.5V-2V input common-mode range using a 40µA tail current. Designed transistor-level bias circuits (Vbp1, Vbp2, Vbn1, Vbn2) and evaluated PSRR, CMRR, and transient response, ensuring high slew rate and stable operation.
- AC and Transient Analysis: Conducted gain vs. frequency and phase margin simulations across input common-mode levels, ensuring compliance with design specifications. Generated PSRR+, PSRR-, and CMRR plots and evaluated transient response for a 1kHz signal with a 10ms time span.

Design and Analysis of a Single Ended NMOS Input Folded Cascode Amplifier with a class AB output buffer circuit:

- Specifications: Supply voltage of 3V, ensuring high linearity, low power, and stable performance for analog signal processing.
- Design Features: Achieved 2mW power dissipation, 1V peak-to-peak output swing with a 1kΩ load, HD3≥50dB at 5kHz, 10V/µs slew rate, 10MHz unity gain bandwidth, 60° phase margin, and PSRR/CMRR of 80dB at 10kHz. The design ensures a 10nV/Hz noise floor and 90dB open-loop DC gain with a 200pF load.
- Performance Analysis: Conducted stability analysis across Process, Voltage, and Temperature Corners, ensuring compliance with gain, noise, and phase margin specifications..

Design and Analysis of a ß-multiplier based constant gm current reference:

- Specifications: Designed a β-multiplier for constant gm, ensuring stable biasing across 2.0V-3.0V supply.
- Design Features: Implemented three variations of ß-multiplier based circuits to achieve reference currents of 10µA, optimized for minimal variation with process, voltage, and temperature. Integrated start-up circuits to ensure reliable operation.
- Performance Analysis: Conducted detailed simulations to evaluate reference current matching within ± 5% for a wide VDD range. Validated constant gm behavior in biased transistors with less than ± 5% variation across temperatures from -20°C to +85°C.

Design and Analysis of Low Dropout Voltage Regulator:

- Specifications: Designed a low dropout voltage regulator with VDD = 2.2V, to provide a regulated voltage output of 1.6V and PDC < 0.3mW.
- Design Features: Implemented an Operational Transconductance Amplifier (OTA) based error amplifier, achieved LDO load capability ranging from 1mA to 50mA.
- AC Analysis: Conducted stability analysis across Process, Voltage, and Temperature Corners to achieve 40 dB Open Loop Gain and 60 degree Phase Margin with BW > 200KHz while driving 10pF load.

Design and Analysis of Two Stage Compensated Amplifier using Current Mirror Biasing:

- Specifications: Vdd = 2V, Power consumption < 1mW, Gain ≥ 70dB, Output Swing ≥ 1.3Vpp.
- AC Analysis: Conducted AC simulations to plot gain vs. frequency, phase vs. frequency, and to achieve 60 degree Phase Margin.
- Transient Analysis: Assessed the maximum input signal amplitude for linear output and swing to ensure distortion-free operation.

Design and Analysis of 5 transistor OTA with Active PMOS Load using Current Mirror Biasing:

- Specifications: Vdd = 1.6V, Ivdd < 170uA, Gain ≥ 33dB, Output Swing ≥ 1.2Vpp, Bandwidth > 2.5MHz.
- AC Analysis: Conducted AC simulations across Process, Voltage, and Temperature variations to verify stability in differential and common-mode gain and phase vs. frequency to achieve 40 dB Gain Margin and 60 degree Phase Margin. Additionally analyzed CMRR and PSRR (both positive and negative) vs frequency to ensure robust noise rejection and power supply rejection.

Design and Analysis of Wide Swing Single Stage Cascode Amplifier using Current Mirror Biasing:

- Specifications: Ids < 0.5mA, Power Consumption < 1mW, Gain ≥ 30dB, Output Swing ≥ 1.6V, Bandwidth > 3MHz.
- AC Analysis: Conducted AC simulations to plot gain vs. frequency, phase vs. frequency, and determined the 3dB bandwidth for performance evaluation.
- Transient Analysis: Assessed maximum input signal amplitude for linear output and swing to ensure distortion-free operation.

Design and Analysis of Common Source Amplifier:

- Specifications: Designed a common source (CS) amplifier with a drain current of 200 μA, overdrive voltage of 0.2 V, and a W/L ratio of 20 using minimum gate length technology.
- Simulation Analysis: Analyzed Id vs Vds, Id vs Vgs, Vout vs Vin, Gain vs Frequency, Phase vs Frequency, and 3dB bandwidth

Professional Experience

ROHM Semiconductor India Pvt Ltd (Bangalore, KA, India) October 2021 – July 2024

A Japanese electronic parts manufacturer based in Kyoto, Japan.

Backend Verification Engineer-1

Responsible for developing a Test Plan, bench characterization, quality analysis tests, and IC Validation.

- **Design Specification Interpretation and Test Plan Creation:-** Collaborated with cross-functional design teams on automotive IC projects to thoroughly understand the functionality and requirements specific to vehicle applications. Translated detailed design specifications into comprehensive test plans to ensure rigorous validation against industry standards and robust performance under various conditions. This process included identifying critical parameters, defining test methodologies, and aligning on validation objectives with stakeholders.
- **Lab Instrumentation and Measurement:-** Operated and maintained advanced lab instruments, including oscilloscopes, power supplies, thermal chambers, electronic loads, and current sources, to perform precise measurements and testing. Conducted in-depth tests on devices, analyzing real-time data to assess performance metrics, detect anomalies, and ensure compliance with design expectations. This involved setting up complex measurement configurations and ensuring consistent calibration of equipment for accurate results.
- **Comprehensive DUT Characterization Across PVT Corners:-** Performed detailed characterization of Devices Under Test (DUT) across various process, voltage, and temperature (PVT) corners to evaluate performance robustness. This included running test scripts, collecting data, and analyzing results to assess operational integrity under worst-case scenarios. The analysis ensured the DUT met functional specifications and adhered to stringent quality standards required for automotive applications.
- **Lab Automation and Communication Development:-** Developed and implemented automation solutions using Python and KICKSTART to optimize testing efficiency. Created scripts to enable USB and LAN-based communication for automating test sequences and handling large data-sets. This reduced manual intervention, minimized testing time, and improved accuracy in repetitive testing scenarios, facilitating faster validation cycles.
- **Quality Analysis for High Yield Assurance:-** Conducted rigorous quality analysis on DUTs, performing statistical yield analysis and verifying adherence to automotive-grade reliability and performance standards. These tests focused on identifying potential failures, ensuring device consistency, and providing actionable feedback for process improvements.
- **Design for Testability (DFT) Process Documentation:-** Documented Design for Testability (DFT) processes for upcoming projects, focusing on enhancing test coverage and simplifying fault diagnosis. This included creating detailed guides for test implementation, ensuring better fault coverage, and enabling efficient debugging during silicon validation.

Technical Extracurricular Activities :-

Formula Bharat & Formula Green [Part of Formula Student Team] (2018-2021):

Contributed to the design, simulation, and testing of electric vehicle systems, focusing on power-train optimization, battery management circuit design, motor control algorithms, energy-efficient design, and the integration of panel logic for real-time performance monitoring and analysis.