Yu (Kevin) Cao

Professor, Electrical Engineering
Affiliated Professor, Computer Science and Engineering

School of Electrical, Computer and Energy Engineering, Arizona State University
P.O. Box 875804, Tempe, AZ 85287-5804
Office: 480-965-1472; Fax: 480-727-9209
E-mail: ycao@asu.edu; http://nimo.asu.edu/ycao

Education

1997 – 2002 University of California, Berkeley, CA, USA
Ph.D. in Engineering – EECS (December 2002)
Dissertation: *Nanometer Circuit Performance Analysis: Device and Interconnect*

M.A. in Biophysics (December 1999)

1991 – 1996 Peking University, Beijing, China
B.S. in Physics (July 1996)

Work Experience

2015 – Professor, School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

2013 – 2014 Visiting Associate Professor, Graduate School of Informatics, Kyoto University, Kyoto, Japan

2009 – 2015 Associate Professor, School of ECEE, ASU, Tempe, AZ

2004 – 2009 Assistant Professor, School of ECEE, ASU, Tempe, AZ

2003 – 2004 Post-Doctoral Researcher, University of California, Berkeley, CA
Berkeley Wireless Research Center, Advisor: Professor Jan M. Rabaey

1999 – 2002 Graduate Student Researcher, University of California, Berkeley, CA
Device Group, Department of EECS, Advisor: Professor Chenming Hu

2001 Summer Research Intern, IBM Microelectronics Division, Hopewell Junction, NY

2000 Summer Research Intern, Hewlett-Packard Laboratories, Palo Alto, CA

Teaching Experience

- EEE 333: HDL and Programmable Logic
- EEE 425: Digital Systems and Circuits
- EEE 525: VLSI Design
- EEE 598: Modeling and Design Solutions for Nano-CMOS Technology (Developed)

Honors and Awards

2017 IEEE Fellow, "for development of predictive technology models for reliable circuit and system integration"

2016 Top 5% Teaching Award, Ira. A. Fulton Schools of Engineering, ASU

2015	Top 5% Teaching Award, Ira. A. Fulton Schools of Engineering, ASU
2013	Top 5% Teaching Award, Ira. A. Fulton Schools of Engineering, ASU
2012	Best Paper Award, IEEE Computer Society Annual Symposium on VLSI
2012	Top 5% Teaching Award, Ira. A. Fulton Schools of Engineering, ASU
2010	Top 5% Teaching Award, Ira. A. Fulton Schools of Engineering, ASU
2009	ACM SIGDA Outstanding New Faculty Award
2009	Promotion and Tenure Faculty Exemplar, Arizona State University
2009	Distinguished Lecturer of the IEEE Circuits and Systems Society (CAS)
2008	Chunhui Award for Outstanding Oversea Chinese Scholars, China
2007	Best Paper Award, International Symposium on Low Power Electronics and Design
2007	IBM Faculty Award
2006	NSF Faculty Early Career Development (CAREER) Award
2006	IBM Faculty Award
2004	Best Paper Award, International Symposium on Quality Electronic Design
2000	Beatrice Winner Award, International Solid-State Circuits Conference
1997	Biophysics Graduate Program Fellowship, University of California, Berkeley
1996	Regents Fellowship, University of California, Santa Cruz

Research Interests

- Predictive modeling of nanoelectronic devices
- Physical-level design and tools for variability and reliability
- Reliable integration of CMOS and emerging technologies
- Neural-inspired hardware and algorithms for learning

Teaching Interests

- Undergraduate: VLSI design and synthesis, solid-state devices, digital circuits and systems, analog integrated circuits, computer architecture
- Graduate: VLSI design for nanoscale technology, device modeling, computer-aided design

Professional Service

- Guest Editor, *ACM Journal on Emerging Technologies in Computing Systems*, Special Issue on Hardware and Algorithms for Learning On-a-chip, 2016
- Guest Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* Special Issue on Cross-layer Reliability and Security, 2016
- Guest Editor, *IEEE Transactions on Nanotechnology*, Special Issue on Nanoelectronic Devices and Circuits for Next Generation Sensing and Information Processing, 2016
- Advisory Board Member, International Membrane Computing Society (IMCS), 2016
- Chair, Digital Design, Timing and Simulation Sub-Committee, *Design Automation Conference* (DAC), 2016, 2017
- Chair, Circuit Reliability Committee, *IEEE International Reliability Physics Symposium* (IRPS), 2016
- Chair of *Workshop on Hardware and Algorithms for Learning On-a-chip* (HALO), 2015, 2016
- Chair of *Workshop on Adaptive Learning On-a-chip: Hardware and Algorithms* (ALOHA) at *SIAM International Conference on Data Mining*, 2015.

- Co-organizer, Special Session on Cross-layer Technology and Design Solutions for Resilience, *IEEE International Symposium on Circuits and Systems* (ISCAS), 2015
- Chair, Simulation and Modeling Committee, *IEEE Custom Integrated Circuits Conference* (CICC), 2014, 2015
- Co-organizer, Special Session on Toward On-Chip Cortical Computing, *Design Automation Conference* (DAC), 2014
- Co-chair, Circuit Aging/Simulation and Circuit Reliability Committee, *IEEE International Reliability Physics Symposium* (IRPS), 2014
- Co-organizer, Special Session on Neuron Inspired Computing using Nanotechnology, *Asia and South Pacific Design Automation Conference* (ASP-DAC), 2014
- Co-chair, Simulation and Modeling Committee, *IEEE Custom Integrated Circuits Conference* (CICC), 2013
- Chair, Circuit Reliability Committee, *IEEE International Reliability Physics Symposium* (IRPS), 2013
- Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 2012 – present
- Co-organizer, Tutorial on Overcoming CMOS Reliability Challenges: From Devices to Circuits and Systems, *Design, Automation & Test in Europe* (DATE), 2011
- Chair, Signal Integrity and Reliability Sub-Committee, *Design Automation Conference* (DAC), 2010
- Chair, ACM SIGDA Design for Manufacturability Technical Committee, 2010
- Associate Editor, *Journal of Computational Electronics*, Springer, 2010 – 2013
- Program Chair, *1st IEEE CASS Summer School on Physical Design of Reliable Systems*, Brazil, 2010
- Guest Editor, *IEEE Design & Test of Computers*, Special Issue on Compact Variability Modeling, 2010
- Chair, Circuit Reliability Committee, *IEEE International Reliability Physics Symposium* (IRPS), 2010
- Vice Chair, ACM SIGDA Design for Manufacturability Technical Committee, 2009
- Editorial Board, *ASP Journal of Low Power Electronics*, 2009 – present
- Guest Editor, *IEEE Design & Test of Computers*, Special Issue on Design for Reliability, 2009
- Chair, VLSI Circuit and Architecture Track, *IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), 2009
- Organizer, Tutorial on Circuit Reliability, *Asia and South Pacific Design Automation Conference* (ASP-DAC), 2009
- Co-chair, Circuit Reliability Committee, *IEEE International Reliability Physics Symposium* (IRPS), 2009
- Co-organizer of *IEEE/ACM Workshop on Compact Variability Modeling* (CVM), 2008 – 2012
- Chair, Device Modeling and Simulation Subcommittee, *IEEE International Conference on Computer-Aided Design* (ICCAD), 2008
- Chair, Design Contest, *ACM/IEEE International Symposium on Low Power Electronics Design* (ISLPED), 2008 – 2009
- Member of the Compact Modeling Technical Committee, IEEE Electron Devices Society, 2007 – present
- Publicity Chair, IEEE Solid-State Circuits Society, Phoenix Chapter, 2006 – 2008
- Technical Program Committee member:
  - *IEEE Custom Integrated Circuits Conference* (CICC), 2012 – present
  - *ACM/IEEE Design Automation Conference* (DAC), 2007 – 2009, 2016
  - *IEEE Workshop on Design for Reliability and Variability* (DRV), 2009
  - *IEEE Great Lakes Symposium on VLSI* (GLSVLSI), 2006 – 2010
  - *ACM/IEEE International Conference on Computer-Aided Design* (ICCAD), 2005 – 2008, 2014 – present

  - *IEEE International Conference on Computer Design* (ICCD), 2005 – 2007
  - *IEEE International Conference on Microelectronic Test Structures* (ICMTS), 2014 – present
  - *IEEE International Conference on Solid-State and Integrated Circuit Technology* (ICSICT), 2014
  - *IEEE International Electron Devices Meeting* (IEDM), 2011 – 2012
  - *IEEE International Symposium on Nanoelectronic and Information Systems* (iNIS), 2015 – present
  - *IEEE International On-Line Testing Symposium* (IOLTS), 2009 – 2011, 2013
  - *IEEE International Reliability Physics Symposium* (IRPS), 2009 – present
  - *ACM/IEEE International Symposium on Low Power Electronics Design* (ISLPED), 2005 – 2009, 2013 – 2015
  - *IEEE International Symposium on Quality Electronic Design* (ISQED), 2008, 2016
  - *IEEE Computer Society Annual Symposium on VLSI* (ISVLSI), 2009
  - *International Workshop on Compact Modeling* (IWCM), 2012 – present
  - *IEEE/ACM International Symposium on Nanoscale Architectures* (NANOARCH), 2016
  - *ACM/IEEE International Workshop on System Level Interconnect Prediction* (SLIP), 2007 – 2011
- Session Chair, ASP-DAC 2014, CICC 2012/2013, DAC 2005/2007/2009/2013, ICCAD 2005/2006, ICCD 2005, IEDM 2012, IRPS 2010/2013, ISLPED 2005/2007, ISQED 2006, SLIP 2010
- Proposal reviewer for:
  - National Science Foundation
  - Natural Sciences and Engineering Research Council (NSERC) of Canada
  - Research Grants Council (RGC) of Hong Kong
  - University of Arizona ADVANCE program
  - University of California MICRO program
- Reviewer for:
  - *IEEE Computer Architecture Letters, IEEE Transactions on Automation Sciences and Engineering, IEEE Transactions on Computer-Aided Design, IEEE Transactions on Device and Materials Reliability, IEEE Transactions on Electron Devices, IEEE Journal of Solid-State Circuits, IEEE Transactions on VLSI Systems, IEEE Electron Device Letters, IEEE Transactions on Circuits and Systems, IEEE Circuits and Devices Magazine, IEEE Transactions on Nanotechnology*
  - *ACM Transactions on Design Automation of Electronic Systems, ACM Journal of Emerging Technologies in Computing Systems*
  - *AIP Journal of Applied Physics*
  - *ASP Journal of Low Power Electronics*
  - *IBM Journal of Research and Development*
  - *IEE Proceedings of Circuits, Devices and Systems, IET Microwaves, Antennas & Propagation, IET Electronics Letters*
  - *Elsevier Microelectronics Journal, Elsevier Microelectronics Reliability, Elsevier Solid State Electronics, Elsevier VLSI Integration*
  - *Morgan Kaufmann Publishers Inc.*
  - *Springer Journal of Computational Electronics, Springer Journal of Electronic Testing*
  - *Springer Science+Business Media, LLC*

University Service

- ECEE Faculty Search Committee, 2013
- Grand Challenge Scholar Program Faculty Advisory Committee, 2012 – present
- Solid-State Circuits Master (MSE) graduate advisor, 2005 – present
- Curriculum development of the Solid-State Circuits group at ASU, 2005 – present

Consulting Experience

- PetVocal LLC, 2016 – present
- Pepper Hamilton LLP, 2014
- Proplus Design Solutions Inc., San Jose, CA [Technical Advisory Board member, 2011 – present]
- Anova Solutions Inc., Santa Clara, CA, 2005 – 2006
- APIC Corporation, Culver City, CA, 2009
- Rio Design Automation Inc., Santa Clara, CA, 2003 – 2004
- Seiko EDA Technologies Inc., Japan, 2002 – 2003
- Celestry Design Technologies Inc., San Jose, CA, 2001 – 2002

Grants and Contracts

- Intel, "Neuromorphic architecture with distributed inhibition for hierarchical learning and classification," co-PI with Jae-sun Seo and Chaitali Chakrabarti, ASU, 12/01/16 – 11/30/17 [Gift]
- Boehringer Ingelheim, "Asthma control / cough assessment with smart wearable systems," 07/01/16 – 12/31/16
- Defense Advanced Research Projects Agency, "Integrity and reliability of integrated circuits (IRIS)," co-PI with Boeing, 04/01/16 – 09/30/17
- Charles Stark Draper Laboratory, "A mixed-mode hardware platform for spiking neural networks," 01/01/16 – 06/30/17
- Samsung Advanced Institute of Technology (SAIT), "Design low power hardware accelerator for bio-signal processing," co-PI with Sarma Vrudhula, Jingrui He, Jae-sun Seo, ASU, 05/01/15 – 03/01/16, $120,000
- MaxLinear, Inc., "28nm Age Model Development," 08/01/14 – 07/31/15 [Gift]
- MaxLinear, Inc., "28nm Age Model Development," 07/01/13 – 12/31/14 [Gift]
- Center for Embedded Systems, a National Science Foundation's Industry/University Cooperative Research Center, "Design of Ultra-low Power Circuits for Compressive Sensing in Mobile Device," co-PI with Sarma Vrudhula, 07/25/14 – 07/24/15
- National Science Foundation, "CSR: Small: Heterogeneous Memory Design: Exploiting Device Diversity for Superior System Performance," co-PI with Chaitali Chakrabarti, 09/01/12 – 08/31/15
- Defense Advanced Research Projects Agency, "Techniques for Estimating Reliability in COTS ICs (TERCI)," co-PI with Michael Fritze, USC, 07/21/11 – 07/20/14
- Intel Corporation, University Research Office, seed funding to support research on reconfigurable analog design, 01/11 – 12/13 [Gift]
- Intel Corporation, University Research Office, Resilient Computing Program, 01/12 – 12/13 [Gift]
- National Science Foundation, "SHF: Small: Collaborative Research: Fast Sign-Off of Nanoscale Memory: From Predictive Device Modeling to Statistical Circuit Synthesis," 08/15/10 – 07/31/13
- National Science Foundation, "EAGER: Low-Power VLSI Applications of Neuromorphic Circuit Construction with Nanoelectronic Devices," co-PI with Bertan Bakkaloglu, ASU, 09/01/09 – 08/31/10
- Focus Center Research Program (FCRP), IFC, "Scalable Technology Models for Alternative Devices and Interconnect," 11/01/09 – 10/31/10
- Qualcomm, "Benchmarking Nanoscale Circuit Design with Predictive Technology Model," 04/01/08 – 03/31/09
- National Science Foundation, "Self-Assembled Inductors: A New Paradigm in Nanoelectronics Design," co-PI with Hongbin Yu, Bertan Bakkaloglu, Hao Yan, ASU, 09/01/07 – 08/31/10
- Semiconductor Research Corporation, "Predictive Modeling and Simulation of Reliability Degradation in Nanoscale Circuits," 07/01/07 – 06/31/10

- Qualcomm, "Benchmarking Nanoscale Circuit Design with Predictive Technology Model," 04/01/07 – 03/31/08
- Focus Center Research Program (FCRP), GSRC, "System Performance Prediction for Reliable Nanoscale Integration," 09/01/06 – 8/31/09
- Focus Center Research Program (FCRP), MSD-C2S2, "Predictive Technology Modeling for End-of-the-Roadmap and Post-Silicon Technologies," 09/01/06 – 8/31/09
- National Science Foundation, "CAREER: Bridging the Technology-EDA Gap through Strategic Tools for Robust Nanometer Design," 08/15/06 – 07/31/11
- IBM Corporation, Faculty Award for research on nanoelectronic design, 2007 [Gift]
- Semiconductor Research Corporation, "Benchmarking Nanoscale Circuit Reliability with Predictive Technology Models," 09/01/05 – 12/31/06
- IBM Corporation, Faculty Award for research on reliable system design, 2006 [Gift]
- Intel Corporation, funding to support research on variation modeling and analysis, 2006 [Gift]
- Connection One, a National Science Foundation's Industry/University Cooperative Research Center, "Ultra Low-Power Digital Logic Design for Nanometer Technology," 07/01/05 – 09/30/06
- Microelectronics Advanced Research Corporation (MARCO), MSD-C2S2, "Predictive Technology Modeling for Robust Nanometer Design," 04/16/05 – 12/31/06
- Semiconductor Research Corporation, "Robust Low Power Circuit Design with Predictive Technology Models," co-PI with Lawrence Clark, ASU, 01/01-05 – 01/31/06

Students

Ph.D. Graduate Students

- Xiaocong Du
- Abinash Mohanty
- Devyani Patra
- Zihan Xu
- Naveen Suda (December 2015, Dissertation "Reconfigurable architectures and systems for IoT applications," now with ARM)
- Ketul Sutaria (November 2014, Dissertation "Modeling and simulation tools for aging effects in scaled CMOS design," now with Intel)
- Anupama Subramaniam (November 2012, Dissertation "Efficient circuit analysis under multiple input switching," now with Intel)
- Jyothi Velamala (November 2012, Dissertation "Compact modeling and simulation for digital circuit aging," now with Intel)
- Saurabh Sinha (November 2011, Dissertation "Neuromorphic controller for low power systems: from devices to circuits," now with ARM)
- Chi-Chao Wang (March 2011, Dissertation "Predictive modeling for extremely scaled CMOS and post-silicon devices," now with Intel)
- Yun Ye (April 2011, Dissertation "Modeling and simulation of variations in nano-CMOS design," now with Siemens Corporate Technology)
- Min Chen (May 2010, Dissertation "Design for reliability: from silicon characterization, model calibration, to efficient simulation," now with Qualcomm)
- Wei Zhao (March 2009, Dissertation "Predictive technology modeling for scaled CMOS design," now with Qualcomm)
- Wenping Wang (June 2008, Dissertation "Circuit aging in scaled CMOS design: modeling, simulation, and prediction," now with Qualcomm)

- Asha Balijepalli (co-advised with Prof. Trevor Thornton, December 2007, Dissertation "Compact modeling and applications of a PD SOI MESFET," now with GLOBALFOUNDRIES)

Masters Graduate Students

- Srivatsava Gorthy
- Ankita Bansal (June 2016, Thesis "Reliability issues and design solutions in advanced CMOS design," now with Intel)
- Pei An (November 2013, Thesis "Reliable arithmetic circuit design inspired by SN P systems," now with Supertex)
- Venkatesa Sarma Ravi (February 2013, Thesis "Statistical characterization and decomposition of SRAM cell variability and aging," now with Samsung)
- Cheng Xu (November 2012, Thesis "Programmable analog device array (PANDA): a methodology for transistor-level analog emulation," now with Microchip)
- Rui Zheng (April 2011, Thesis "Aging predictive models and simulation methods for analog and mixed-signal circuits," now with Loongson)
- Jia Ni (May 2010, Thesis "Rigorous extraction of V_{th} variation in SRAM cell transistors," now with Bloomberg)
- Varsha Balakrishnan (November 2009, Thesis "Circuit aging simulation for digital and analog circuits," now with Apple)
- Dinesh Ganesan (December 2007, Thesis "Finite point gate model," now with Freescale)
- Ritu Singal (September 2007, Thesis "Compact modeling of non-rectangular gate effect," now with Intel)
- Rakesh Vattikonda (July 2007, Thesis "Predictive modeling of NBTI effect," now with Qualcomm)
- Tarun Sairam (July 2006, Thesis "Low-power digital design with FinFET technology," now with Oracle)

Visiting Scholars

- Zhiming Yang (04/16 – 03/17, Harbin Institute of Technology)
- Yao Ma (09/12 – 08/13, Sichuan University, "Compact modeling of CMOS devices during swift heavy ion irradiation")

Selected Invited Talks and Presentations

- IEEE CEDA Workshop on Design Automation Futures, "CMOS or emerging devices: Technology and design benchmarking for efficient neuromorphic computing," Fremont, CA, October 2016.
- IBM, "Neuromorphic computing on-a-chip: Devices, circuits and algorithms," Yorktown Heights, NY, October 2016.
- Embedded Systems Week, Tutorial, "Algorithms and hardware for learning on-a-chip," Pittsburgh, PA, October 2016.
- International Conference on Field-Programmable Logic and Applications, Tutorial, "Energy-efficient acceleration for neuro-inspired computing on-a-chip," Lausanne, Switzerland, August 2016.
- International Roadmap for Devices and Systems, NanoCrossbar Workshop, "Neuromorphic computing with resistive synaptic arrays: devices, circuits, and systems," Sunnyvale, CA, July 2016.
- Neuromorphic Computing Workshop at Oak Ridge National Laboratory, "Efficient neuromorphic learning with motifs of feedforward inhibition," Oak Ridge, TN, June 2016.
- SIGDA Design Automation Summer School, "Hardware efficiency in neuromorphic computing: devices, circuits, and algorithms," Austin, TX, June 2016.
- Peking University, "Efficient neuromorphic computing on-a-chip: devices, circuits, and algorithms," Beijing, China, May 2016.

- Raytheon Information Systems and Computing Symposium, "Efficient and accurate neuromorphic learning with the feedforward motif," Tucson, AZ, May 2016.
- International Symposium on Quality Electronic Design, "Neuromorphic computing with resistive synaptic arrays: devices, circuits and systems," Santa Clara, CA, March 2016.
- Boehringer Ingelheim, "Asthma control and cough assessment with smart wearable systems," Ingelheim, Germany, March 2016.
- Great Lakes Symposium on VLSI, "On-chip sparse learning with resistive cross-point array architecture," Pittsburgh, PA, May 2015.
- Samsung, "On-chip Learning with Resistive Cross-point Array," San Jose, CA, July 2014.
- Qualcomm, "On-chip Learning with Resistive Cross-point Array," San Diego, CA, July 2014.
- Government Microcircuit Applications & Critical Technology Conference, Tutorial, "Compact Modeling of Circuit Reliability," Charleston, SC, March 2014.
- Samsung Technology Forum, "Designing Smarter SoCs for Reliability," Milpitas, CA, September 2013.
- IEEE Electron Device Society Mini-colloquium, "Hierarchical Exploration of Heterogeneous Memory Design," Peking University, Beijing, China, July 2013.
- Design Automation Conference, Tutorial, "The Roadmap of Unreliability: A Digital Perspective," Austin, TI, June 2013.
- MaxLinear, "The Roadmap of Device Unreliability," San Diego, CA, April 2013.
- International Reliability Physics Symposium, Panelist, "Emerging Trends & Scaling in Reliability," Monterey, CA, April 2013.
- IEEE SSCS Phoenix Chapter / Connection One Research Center, "Designing Smarter SoCs for Reliability," Arizona State University, Tempe, AZ, March 2013.
- ARM, "Hierarchical Memory Modeling for Resilient Integration," San Jose, CA, December 2012.
- International Conference on Solid-State and Integrated Circuit Technology, "Multi-level Reliability Simulation for IC design," Xian, China, October 2012.
- IEEE Electron Device Society Mini-colloquium, "Circuit Reliability Modeling and Simulation for Complex SoCs," Peking University, Beijing, China, October 2012.
- CMOS Emerging Technologies, "Design Exploration of Heterogeneous Memory Technologies," Vancouver, Canada, July 2012.
- Workshop on Compact Modeling, Nanotech Conference & Expo 2012, "Hierarchical Memory Modeling for Reliable Integration," Santa Clara, CA, June 2012.
- International Reliability Physics Symposium, Tutorial, "Circuit Reliability Modeling and Simulation for Complex SoCs," Anaheim, CA, April 2012.
- Workshop on Compact Modeling, Nanotech Conference & Expo 2011, "A Universal Memory Model for Design Exploration," Boston, MA, June 2011.
- 219th Electrochemical Society Meeting, "Intrinsic Variability and Reliability in Nano-CMOS," Montreal, Canada, May 2011.
- International Reliability Physics Symposium, Year in Review, "Circuit Reliability: Cross-layer Resilience Challenges and Solutions," Monterey, CA, April 2011.
- IBM, Austin Distinguished Seminar Series, "Design at the End of the Silicon?" Austin, TX, April 2011.
- Design, Automation and Test in Europe, Tutorial, "Modeling & Simulation of CMOS Circuit Reliability," Grenoble, France, March 2011.
- International Electron Devices Meeting, "Intrinsic Variability in Nano-CMOS Design and Beyond," San Francisco, CA, December 2010.
- Intel, "Programmable ANalog Device Array (PANDA): A Platform for Transistor-Level Analog Reconfigurability," Santa Clara, CA, November 2010.

- Workshop on Simulation and Characterization of Statistical CMOS Variability and Reliability, International Conference on Simulation of Semiconductor Processes and Devices, "Statistical Reliability Modeling and Characterization in Scaled CMOS Design," Bologna, Italy, September 2010.
- International Workshop on System Level Interconnect Prediction, Panelist, "New Models and Algorithms for Multi-core Interconnects," Anaheim, CA, June 2010.
- TI, "Modeling and Simulation of Digital Circuit Reliability," Dallas, TX, June 2010.
- First International Variability Characterization Workshop, "Predictive Variability Model," Hsinchu, Taiwan, April 2010.
- Semiconductor Research Corporation (SRC) Technology Transfer e-Workshop, "In-Situ Characterization and Modeling of Circuit Reliability in Dynamic Operations," March 2010.
- First IEEE CASS Summer School on Physical Design of Reliability Circuits, "Variability and Reliability in Advanced CMOS Design: Modeling and Resilient Design Solutions," Porto Alegre, Brazil, January 2010.
- CMOS Emerging Technologies Workshop, "Compact Variability Modeling of Nanoscale CMOS Technology," Vancouver, Canada, September 2009.
- Air Force Research Lab, Technology Seminar, "Reliability in Advanced CMOS Design: Modeling and Resilient Solutions," Albuquerque, NM, August 2009.
- GLOBALFOUNDRIES, "Modeling and Design of Reliable Nanoelectronics," Sunnyvale, CA, July 2009.
- Intel, Pathfinding Forum, "Predictive Variability Modeling and Design Implications," Santa Clara, CA, July 2009.
- IBM, "Compact Variability Modeling and Design Implications," Yorktown Heights, NY, April 2009; Austin, TX, June 2009.
- Asia and South Pacific Design Automation Conference, Tutorial, "Circuit Reliability: Modeling, Simulation, and Resilient Design Solutions," Yokohama, Japan, 2009.
- IEEE Workshop on Design for Reliability and Variability, "Modeling and Simulation Tools for Resilient Nanoelectronic Design," Santa Clara, CA, October 2008.
- Intel, "Predictive Technology Modeling for Robust Nanoelectronic Design: CMOS and Beyond" and "Modeling and Diagnosis of Circuit Reliability in Scaled CMOS Design," Hillsboro, OR, August 2008.
- International On-Line Testing Symposium, Invited Talk, "Modeling and Simulation of Circuit Aging in Scaled CMOS Design," Rhodes, Greece, July 2008.
- International Reliability Physics Symposium, Tutorial, "Reliability Modeling and Simulation for Sub-45nm Design," Phoenix, AZ, April 2008.
- ARM, "Reliable Integration with Unreliable Nanoscale Devices: Predictive Modeling and Design Solutions," Sunnyvale, CA, March 2008.
- DARPA/MTO LIBRA Workshop on Designing Reliable Systems from Unreliable Components, "Reliable Modeling and Tools for Resilient Design," Arlington, VA, November, 2007.
- University of Washington, Department of Electrical Engineering, Research Colloquium, "Predictive Technology Model for Nanoelectronic Design," Seattle, WA, November 2007.
- International Conference on Computer-Aided Design, embedded tutorial, "MOSFET Modeling for 45nm and beyond," November, 2007.
- Tsinghua University and Southeast University, "Predictive Technology Modeling in the Nanoelectronics Era," China, May 2007.
- Intel, "Coping with Process Variations in Circuit Modeling and Simulation," Santa Clara, CA, February, 2007.
- IBM, "Predictive Modeling of NBTI Effects for Reliable Nanoscale Design," Austin, TX, February 2007.

- Synopsys Engineering Seminar Series (SESS), "Predictive Technology Modeling for Robust Circuit Design with Nano-CMOS and Post-Silicon Technologies," Sunnyvale, CA, December 2006.
- University of California, Los Angeles, "Bridging Nanometer to Gigascale: Predictive Technology Modeling for Robust IC Design," November 2006.
- TI, "Predictive Modeling of Variability and Reliability in Nanoscale Design," Dallas, TX, November 2006.
- Qualcomm, "Benchmarking Nanoscale Circuit Design with Predictive Design Model," San Diego, CA, October 2006.
- International Conference on Nano-Networks, "Predictive Technology Model for Nano-CMOS Design Exploration," Lausanne, Switzerland, September 2006.
- Synopsys Engineering Seminar Series (SESS), "Coping with Process Uncertainties in Circuit Modeling and Simulation," Sunnyvale, CA, September 2006.
- Semiconductor Research Corporation (SRC) Technology Transfer e-Workshop, "Benchmarking Nanoscale Circuit Reliability with Predictive Technology Models," August 2006.
- Intel External Long-range Research Seminar (ELRS), "Predictive Technology Modeling for Reliable Nanoscale Integration," San Jose, CA, August 2006.
- Tsinghua University and Peking University, "Bridging Nanometer to Gigascale: Predictive Technology Model for Robust Nanometer Integration," Beijing, China, May 2006.
- LSI Logic, "Predictive Technology Model for Robust Nanoscale Integration," Milpitas, CA, March 2006.
- Intel, "Modeling and Simulation of Variability and Reliability Issues for Robust Nanometer Design," Santa Clara, CA, March 2006.
- IBM T. J. Watson Research Center and Austin Research Laboratories, "Modeling and Simulation of Variability and Reliability Issues for Robust Nanometer Design," Yorktown Heights, NY and Austin, TX, February 2006.
- Arizona State University, Center for Solid State Electronics Research (CSSER) Seminar, "Predictive Technology Model for Robust Nanoscale Integration," Tempe, AZ, February 2006.
- Synopsys, "Benchmarking Sub-45nm Circuits Design with Predictive Technology Models," Sunnyvale, CA, January 2006.
- IBM Austin Research Laboratories, "Variability Modeling and Characterization for Robust Nanometer Design," Austin, TX, August 2005.
- Synopsys, "Bridging the Technology-EDA Gap: Variability Modeling and Characterization for Robust Nanometer Design," Sunnyvale, CA, August 2005.
- Intel, "Bridging Nanometer to Gigascale: Process Variation Modeling for Reliable Design," Santa Clara, CA, February 2005.

Professional Membership

- Fellow, Institute of Electrical and Electronics Engineers (IEEE)
- Member, Association for Computing Machinery (ACM)

Patent

- Shimeng Yu, Yu Cao, Jae-sun Seo, Sarma Vrudhula, Jieping Ye, "Resistive cross-point architecture for robust data representation with arbitrary precision," US patent 9466362, October 11, 2016.
- Lawrence Clark, Yu Cao, "Fast parallel test of SRAM arrays," US patent application 2013/0111282, May 2, 2013.

- Xia Li, Wei Zhao, David Bang, Yu Cao, Seung H. Kang, Matthew Nowak, "Predictive modeling of contact and via modules for advanced on-chip interconnect technology," US patent 8483997, July 9, 2013.
- Xia Li, Wei Zhao, Yu Cao, Shiqun Gu, Seung H. Kang, Matthew Nowak, "Predictive modeling of interconnect modules for advanced on-chip interconnect technology," US patent 8429577, April 23, 2013.
- Xia Li, Wei Zhao, Yu Cao, Shiqun Gu, Seung H. Kang, Ming-Chu King, "Via structure integrated in electronic substrate," US patent 8227708, July 24, 2012.
- Norman Chang, Yu Cao, Osamu Samuel Nakagawa, Shen Lin, Weize Xie, "System for improving circuit simulations by utilizing a simplified circuit model based on effective capacitance and inductance values," US patent 6567960, May 20, 2003.

Publications

Books and Book Chapters

[1] K. B. Sutaria, J. B. Velamala, A. Ramkumar, Y. Cao, "Compact modeling of BTI for circuit reliability analysis," Chapter 6, pp. 93-119, in *Circuit Design for Reliability*, Edited by R. Reis, Y. Cao, G. Wirth, Springer, 2015.

[2] C. Yang, Z. Xu, K. Sutaria, C. Chakrabarti, Y. Cao, "Design exploration of heterogeneous memory technologies," Chapter 19, pp. 407-427, in *VLSI: Circuits for Emerging Applications*, Edited by T. Wojcicki, CRC Press, 2014.

[3] G. Wirth, Y. Cao, J. B. Velamala, K. B. Sutaria, T. Sato, "Charge trapping in MOSFETs: BTI and RTN modeling for circuits," pp. 751-782, in *Bias Temperature Instability for Devices and Circuits*, Edited by T. Grasser, Springer, 2014.

[4] K. Sutaria, J. Velamala, V. Ravi, G. Wirth, T. Sato, Y. Cao, "Multilevel reliability simulation for IC design," pp. 719-749, in *Bias Temperature Instability for Devices and Circuits*, Edited by T. Grasser, Springer, 2014.

[5] W. Xu, S. Sinha, H. Wu, T. Dastagir, Y. Cao and H. Yu, "On-chip spiral inductors with integrated magnetic materials," Chapter 17, pp. 439-462, in *Advanced Circuits for Emerging Technologies*, Edited by Kris Iniewski, John Wiley & Sons, Inc., 2012.

[6] W. Wang, V. Reddy, S. Krishnan, Y. Cao, "Compact modeling for NBTI and CHC effects," pp. 40-60, in *Recent Advancements in Modeling of Semiconductor Processes, Circuits and Chip-Level Interactions*, Edited by Rasit Onur Topaloglu and Peng Li, Bentham Science Publishers Ltd., 2011.

[7] Y. Cao, *Predictive Technology Model for Robust Nanoelectronic Design*, Springer, 2011.

[8] S. Sinha, A. Balijepalli, Y. Cao, "Compact modeling of carbon nanotube transistor and interconnects," Chapter 12, pp. 217-236, in *Carbon Nanotubes*, Edited by Jose Mauricio Marulanda, IN-TECH Education and Publishing, 2010.

[9] W. Wang, V. Reddy, V. Balakrishnan, S. Krishnan, Y. Cao, "Statistical prediction of circuit aging under process variations," Chapter 5, pp. 101-122, in *Solid State Circuits Technologies*, Edited by Jacobus W. Swart, IN-TECH Education and Publishing, 2010.

[10] B. Wong, A. Mittal, Y. Cao, and G. Starr, *Nano-CMOS Circuit and Physical Design*, John Wiley & Sons, Inc., 2004.

Journal Papers

[1] C. Yang, M. Mao, Y. Cao, C. Chakrabarti, "Cost-effective design solutions for enhancing PRAM reliability and performance," to be published in *IEEE Transactions on Multi-Scale Computing Systems*.

[2] M. Mao, Y. Cao, S. Yu, C. Chakrabarti, "Optimizing latency, energy, and reliability of 1T1R ReRAM through cross-layer techniques," to be published in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Special Issue on Emerging Memory Technology, Architecture and Applications, vol. 6, no. 3, pp. 352-363, September, 2016.

[3] L. Xia, P. Gu, B. Li, T. Tang, X. Yin, W. Huang, S. Yu, Y. Cao, Y. Wang, H. Yang, "Technological exploration of RRAM crossbar array for matrix-vector multiplication," *Journal of Computer Science and Technology*, China, vol. 31, no. 1, pp. 3-19, January 2016.

[4] N. Suda, J. Suh, N. Hakim, Y. Cao, B. Bakkaloglu, "A 65nm Programmable ANalog Device Array (PANDA) for analog circuit emulation," *IEEE Transactions on Circuits and Systems I*, vol. 63, no. 2, pp. 181-190, February 2016.

[5] A. R. Subramaniam, J. Roveda, Y. Cao, "A finite-point method for efficient gate characterization under multiple input switching," *ACM Transactions on Design Automation of Electronic Systems*., vol. 21, no. 1, article 10, pp. 10.1-10.25, November 2015.

[6] J. Seo, B. Lin, M. Kim, P.-Y. Chen, D. Kadetotad, Z. Xu, A. Mohanty, S. Vrudhula, S. Yu, J. Ye, Y. Cao, "On-chip sparse learning acceleration with CMOS and resistive synaptic devices," *IEEE Transactions on Nanotechnology*, Special Issue on Cognitive and Natural Computing with Nanotechnology, vol. 14, no. 6, pp. 969-979, November 2015.

[7] L. Gao, I-T. Wang, P.-Y. Chen, S. Vrudhula, J. Seo, Y. Cao, T.-H. Hou, S. Yu, "Fully parallel Write/Read in resistive synaptic array for accelerating on-chip learning," *Nanotechnology*, IOP Science, vol. 26-455204, pp. 1-9, November 2015.

[8] K. B. Sutaria, A. Mohanty, R. Wang, R. Huang, Y. Cao, "Accelerated aging in analog and digital circuits with feedback," *IEEE Transactions on Device and Materials Reliability*, vol. 15, no. 3, pp. 384-393, September 2015.

[9] A. Subramaniam, J. Roveda, Y. Cao, "Finite-point method for efficient timing characterization of sequential elements," *Integration, the VLSI Journal*, Elsevier Ltd., vol. 49, pp. 104-113, March 2015.

[10] D. Kadetotad, Z. Xu, A. Mohanty, P.-Y. Chen, B. Lin, J. Ye, S. Vrudhula, S. Yu, Y. Cao, J. Seo, "Parallel architecture with resistive crosspoint array for dictionary learning acceleration," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Special Issue on Solid-State Memristive Devices and Systems, vol. 5, no. 2, pp. 194-204, 2015.

[11] Z. Xu, M. Cavaliere, P. An, S. Vrudhula, Y. Cao, "The stochastic loss of spikes in Spiking Neural P systems: Design and implementation of reliable arithmetic circuits," *Fundamenta Informaticae*, Special Issue on Computational Aspects of Bio-processes, vol. 134, no. 1-2, pp. 183-200, 2014.

[12] Z. Xu, C. Yang, M. Mao, K. Sutaria, C. Chakrabarti, Y. Cao, "Compact modeling of STT-MTJ devices," *Solid-State Electronics*, Elsevier Ltd., Special Issue on the 2013 European Solid-State Device Research & Circuits Conference, vol. 102, pp. 76-81, December 2014.

[13] Z. Xu, A. Mohanty, P.-Y. Chen, D. Kadetotad, B. Lin, J. Ye, S. Vrudhula, S. Yu, J. Seo, Y. Cao, "Parallel programming of resistive cross-point array for synaptic plasticity," *Procedia Computer Science*, Elsevier Ltd., *5th Annual International Conference on Biologically Inspired Cognitive Architectures*, vol. 41, pp. 126-133, November 2014.

[14] C. Yang, Y. Emre, Z. Xu, H. Chen, Y. Cao, C. Chakrabarti, "A low cost multi-tiered approach to improving the reliability of multi-level cell PRAM," *Journal of Signal Processing Systems*, Elsevier Ltd., Special Issue on the 2012 IEEE Workshop on Signal Processing Systems, vol. 76, no. 2, pp. 133-147, August 2014.

[15] K. B. Sutaria, J. B. Velamala, C. Kim, T. Sato, Y. Cao, "Aging statistics based on trapping/detrapping: compact modeling and silicon validation," *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 2, pp. 607-615, June 2014.

[16] Y. Cao, J. Velamala, K. Sutaria, M. S.-W. Chen, J. Ahlbin, I. S. Esqueda, M. Bajura, M. Fritze, "Cross-layer modeling and simulation of circuit reliability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 1, pp. 8-23, January 2014. **[Keynote]**

[17] X. Chen, Y. Wang, Y. Cao, Y. Xie, H. Yang, "Assessment of circuit optimization techniques under NBTI," *IEEE Design & Test*, Special Issue on Variability and Aging, vol. 30, no. 6, pp. 40-49, November/December 2013.

[18] J. B. Velamala, K. B. Sutaria, H. Shimuzu, H. Awano, T. Sato, G. Wirth, Y. Cao, "Compact modeling of statistical BTI under trapping/detrapping," *IEEE Transactions on Electron Devices*, vol. 60, no. 11, pp. 3645-3654, November 2013.

[19] X. Chen, H. Luo, Y. Wang, Y. Cao, Y. Xie, Y. Ma, H. Yang, "Evaluation and mitigation of performance degradation under RTN for digital circuits," *IET Circuits, Devices & Systems.*, Special Issue on Design Methodologies for Nanoelectronic Digital and Analogue Circuits, vol. 7, no. 5, pp. 273-282, September 2013. **[invited]**

[20] S. Yang, W. Wang, M. Hagan, W. Zhang, P. Gupta, Y. Cao, "NBTI aware circuit node criticality computation," *ACM Journal of Emerging Technologies in Computing Systems*, vol. 9, no. 3, pp. 23:1-19, September 2013.

[21] J. B. Velamala, K. B. Sutaria, V. Ravi, Y. Cao, "Failure analysis of asymmetric aging under NBTI," *IEEE Transactions on Device and Materials Reliability*, vol. 13, no. 2, pp. 340-349, June 2013. **[invited]**

[22] J. Suh, N. Suda, C. Xu, N. Hakim, Y. Cao, B. Bakkaloglu, "Programmable analog device array (PANDA): a methodology for transistor-level analog emulation," *IEEE Transactions on Circuits and Systems I*, vol. 60, no. 6, pp. 1369-1380, June 2013.

[23] J. Sun, R. Zheng, J. B. Velamala, Y. Cao, R. Lysecky, K. V. Shankar, J. Roveda, "A self-evolving design methodology for power efficient multi-core systems," *ACM Transactions on Design Automation of Electronic Systems*, Special Issue on Adaptive Power Management for Energy and Temperature Aware Computing Systems, vol. 18, no. 1, pp. 4:1-4:24, December 2012.

[24] X. Chen, Y. Wang, Y. Cao, Y. Ma, and H. Yang, "Variation-aware supply voltage assignment for simultaneous power and aging optimization," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 20, no. 11, pp. 2143-2147, November 2012.

[25] C.-C. Wang, Y. Ye, Y. Cao, "The potential of Fe-FET for robust design under variations: a compact modeling study," *Microelectronics Journal*, Elsevier Ltd., vol. 43, no. 11, pp. 898-903, November 2012.

[26] C. Yang, Y. Emre, Y. Cao, C. Chakrabarti, "Improving reliability of non-volatile memory technologies through circuit level techniques and error control coding," *EURASIP Journal on Advances in Signal Processing*, vol. 2012, no. 211, pp. 1-24, October 2012.

[27] M. Chen, V. Reddy, S. Krishnan, V. Srinivasan, Y. Cao, "Asymmetric aging and workload sensitive bias temperature instability sensors," *IEEE Design & Test of Computers*, Special Issue on On-Chip Structures for Smarter Silicon, vol. 29, no. 5, pp. 18-26, September/October 2012.

[28] A. Subramaniam, R. Singhal, C.-C. Wang, Y. Cao, "Leakage reduction through optimization of regular layout parameters," *Microelectronics Journal*, Elsevier Ltd., vol. 43, no. 1, pp. 25-33, January 2012.

[29] S. Sinha, J. Suh, B. Bakkaloglu, Y. Cao, "Workload-aware neuromorphic design of power controller," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 1, no. 3, pp. 381-390, September 2011.

[30] Y. Ye, F. Liu, M. Chen, S. Nassif, and Y. Cao, "Statistical modeling and simulation of threshold variation under random dopant fluctuations and line-edge roughness," *IEEE Transactions on VLSI Systems*, vol. 19, no. 6, pp. 987-996, June 2011.

[31] E. Mintarno, J. Skaf, R. Zheng, J. Velamala, Y. Cao, S. Boyd, R. W. Dutton, S. Mitra, "Self-tuning for maximized lifetime energy-efficiency in the presence of circuit aging," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 5, pp. 760-773, May 2011.

[32] J. Velamala, C.-C. Wang, R. Zheng, Y. Ye, Y. Cao, "Intrinsic variability and reliability in nano-CMOS," *Electrochemical Society Transactions*, vol. 35, no. 4, pp. 353-367, April 2011. **[invited]**

[33] S. Sinha, J. Suh, B. Bakkaloglu, Y. Cao, "Workload-aware low-power supply voltage controller," *the Neuromorphic Engineer*, 10.2417/1201104.003553, pp. 1-3, April 2011.

[34] Y. Wang, X. Chen, W. Wang, Y. Cao, Y. Xie, H. Yang, "Leakage power and circuit aging cooptimization by gate replacement techniques," *IEEE Transactions on VLSI Systems*, vol. 19, no. 4, pp. 615-628, April 2011.

[35] W. Xu, S. Sinha, H. Wu, M. Dastagir, D. S. Gardner, Y. Cao, H. Yu, "Sub-100 μm scale on-chip inductors with CoZrTa for GHz applications," *Journal of Applied Physics*, vol. 109, no. 7, 07A316, pp. 1-3, April 2011.

[36] W. Xu, S. Sinha, T. Dastagir, H. Wu, B. Bakkaloglu, D. S. Gardner, Y. Cao, and H. Yu, "Performance enhancement of on-chip inductors with permalloy magnetic rings," *IEEE Electron Device Letters.*, vol. 32, no. 1, pp. 69-71, January 2011.

[37] Y. Ye, S. Gummalla, C.-C. Wang, C. Chakrabarti, Y. Cao, "Random variability modeling and its impact on scaled CMOS circuits," *Journal of Computational Electronics*, Springer, vol. 9, pp. 108-113, December 2010. **[invited]**

[38] T. Dastagir, W. Xu, S. Sinha, H. Wu, Y. Cao, and H. Yu, "Tuning the permeability of permalloy films for on-chip inductor applications," *Applied Physics Letter*s, vol. 97, 162506, pp. 1-3, October 2010.

[39] R. Singal, A. Balijepalli, A. Subramaniam, C.-C. Wang, F. Liu, S. Nassif, Y. Cao, "Modeling and analysis of the non-rectangular gate effect for post-lithography circuit simulation," *IEEE Transactions on VLSI Systems*, vol. 18, no. 4, pp. 666-670, April 2010.

[40] Y. Cao, F. Liu, "Compact variability modeling in scaled CMOS design," *IEEE Design & Test of Computers*, Special Issue on Compact Variability Modeling in Scaled CMOS Design, vol. 27, no. 2, pp. 6-7, March/April 2010.

[41] W. Xu, S. Sinha, F. Pan, T. Dastagir, Y. Cao, H. Yu, "Improved frequency response of on-chip inductors with patterned magnetic dots," *IEEE Electron Device Letters*, vol. 31, no. 3, pp. 207-209, March 2010.

[42] W. Wang, S. Yang, S. Bhardwaj, R. Vattikonda, S. Vrudhula, F. Liu, Y. Cao, "The impact of NBTI effect on combinational circuit: modeling, simulation, and analysis," *IEEE Transactions on VLSI Systems*, vol. 18, no. 2, pp. 173-183, 2010.

[43] Y. Cao, A. Balijepalli, S. Sinha, C.-C. Wang, W. Wang, W. Zhao, "The predictive technology model in the late silicon era and beyond," *Foundations and Trends in Electronic Design Automation*, vol. 3, no. 4, pp. 305-401, 2010. **[invited]**

[44] Y. Cao, J. Tschanz, P. Bose, "Reliability challenges in nano-CMOS design," *IEEE Design & Test of Computers*, Special Issue on Design for Reliability at 32nm and Beyond, vol. 26, no. 6, pp. 6-7, November/December 2009.

[45] M. Chen, W. Zhao, F. Liu, Y. Cao, "Finite-point based transistor model: A new approach to fast circuit simulation," *IEEE Transactions on VLSI Systems*, vol. 17, no. 10, pp. 1470-1480, October 2009.

[46] S. Sinha, A. Balijepalli, Y. Cao, "Compact model of carbon nanotube transistor and interconnect," *IEEE Transactions on Electron Devices*, vol. 56, no. 10, pp. 2232-2242, October 2009.

[47] A. Balijepalli, J. Ervin, W. Lepkowski, Y. Cao, and T. Thornton, "Compact modeling of a PD SOI MESFET for wide temperature designs," *Microelectronics Journal*, Elsevier Ltd., vol. 40, no. 9, pp. 1264-1273, September 2009.

[48] W. Zhao, X. Li, S. Gu, S. H. Kang, M. Nowak, Y. Cao, "Field-based capacitance modeling for sub-65nm on-chip interconnect," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, pp. 1862-1872, September 2009.

[49] R. Krishnan, M. Debole, W. Wang, V. Balakrishnan, H. Luo, Y. Wang, Y. Cao, Y. Xie, V. Narayanan, "New-Age: A NBTI-estimation framework for microarchitectural components," *International Journal of Parallel Programming.*, vol. 37, pp. 417-431, May 2009.

[50] W. Zhao, F. Liu, K. Agarwal, D. Acharyya, S. R. Nassif, K. Nowka, Y. Cao, "Rigorous extraction of process variations for 65nm CMOS design," *IEEE Transactions on Semiconductor Manufacturing*, vol. 22, no. 1, pp. 196-203, February 2009.

[51] J. M. Wang, Y. Cao, M. Chen, J. Sun, A. Mitev, and K. Potluri, "Capturing device mismatch in analog and mixed-signal designs," *IEEE Circuits and Systems Magazine.*, vol. 8, no. 4, pp. 37-44, 2008. **[invited]**

[52] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, S. Vrudhula, "A scalable model for predicting the effect of NBTI for reliable design," *IET Circuits, Devices & Systems.*, vol. 2, no. 4, pp. 361-371, 2008.

[53] T. Austin, V. Bertacco, S. Mahlke, Y. Cao, "Reliable systems on unreliable fabrics," *IEEE Design & Test of Computers*, vol. 25, no. 4, pp. 322-332, July/August, 2008. **[invited]**

[54] B. H. Calhoun, Y. Cao, X. Li, K. Mai, L. T. Pileggi, R. A. Rutenbar, and K. L. Shepard, "Digital circuit design challenges and opportunities in the era of nanoscale CMOS," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 343-365, February 2008. **[invited]**

[55] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, Y. Cao, "Compact modeling and simulation of circuit reliability for 65nm CMOS technology," *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 4, pp. 509-517, December 2007. **[invited]**

[56] Y. Cao and L. T. Clark, "Mapping statistical process variations toward circuit performance variability: an analytical modeling approach," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 10, pp. 1866-1873, October 2007.

[57] W. Zhao and Y. Cao, "Predictive technology model for nano-CMOS design exploration," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 3, no. 1, pp. 1-17, April 2007.

[58] H. Qin, R. Vattikonda, T. Trinh, Y. Cao, J. Rabaey, "SRAM cell optimization for ultra-low power standby," *ASP Journal of Low Power Electronics*, vol. 2, no. 3, pp. 401-411, December 2006.

[59] W. Zhao, Y. Cao, "New generation of predictive technology model for sub-45nm early design exploration," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2816-2823, November 2006.

[60] J. He, M. Fang, B. Li, G. Zhang, Y. Cao, "A new analytic approximation to general diode equation," *Solid-State Electronics*, Elsevier Ltd., vol. 50, no. 9, pp. 1371-1374, September 2006.

[61] S. Bhardwaj, Y. Cao, S. Vrudhula, "Statistical leakage minimization of digital circuits using gate sizing, gate length biasing, and threshold voltage selection," *ASP Journal of Low Power Electronics*, vol. 2, no. 2, pp. 240-250, August 2006.

[62] J. Chen, L. T. Clark, and Y. Cao, "Maximum Fan-In/Out: Ultra-low voltage circuit design in the presence of variations," *IEEE Circuits and Devices Magazine*, vol. 21, no. 6, pp. 12-20, November 2005.

[63] Y. Cao, X.-D. Yang, X. Huang, and D. Sylvester, "Switch-factor based loop RLC modeling for efficient timing analysis," *IEEE Transactions on VLSI Systems*, vol. 13, no. 9, pp. 1072-1078, September 2005.

[64] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu, and J. M. Rabaey, "Standby supply voltage minimization for deep sub-micron SRAM," *Microelectronics Journal*, Elsevier Ltd. vol. 36, no. 9, pp. 789-800, September 2005.

[65] Y. Cao, X. Huang, D. Sylvester, T.-J. King, and C. Hu, "Impact of on-chip interconnect frequency-dependent *R(f)L(f)* on digital and RF design," *IEEE Transactions on VLSI Systems*, vol. 13, no. 1, pp. 158-162, January 2005.

[66] R. Chang, Y. Cao, and C. Spanos, "Modeling metal dishing for interconnect optimization," *IEEE Transactions on Electron Devices*, vol. 51, no. 10, pp.1577-1583, October 2004.

[67] Y. Cao, M. Orshansky, D. Sylvester, T. Sato, and C. Hu, "SPICE up your MOSFET modeling: presenting a new paradigm of predictive MOSFET modeling for early circuit design innovation," *IEEE Circuits and Devices Magazine*, vol.19, no. 4, pp. 17-23, July 2003.

[68] T. Sato, Y. Cao, K. Agarwal, D. Sylvester, and C. Hu, "Bidirectional closed-form transformation between on-chip coupling noise waveforms and interconnect delay change curves," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 22, no. 5, pp. 560-572, May 2003.

[69] Y. Cao, R. A. Groves, N. D. Zamdmer, J. Plouchart, R. A. Wachnik, X. Huang, T. King, and C. Hu, "Frequency-independent equivalent circuit model for on-chip spiral inductors," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 419-426, March 2003.

[70] X. Huang, P. Restle, T. Bucelot, Y. Cao, and T. King, "Loop-based interconnect modeling and optimization approach for multi-GHz clock network design," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 457-463, March 2003.

[71] Y. Cao, C. Hu, X. Huang, A. B. Kahng, I. L. Markov, M. Oliver, D. Stroobandt, and D. Sylvester, "Improved a priori interconnect predictions and technology extrapolation in the GTX system," *IEEE Transactions on VLSI Systems*, vol. 11, no. 1, pp. 3-14, February 2003.

[72] Y. Cao, X. Huang, N. Chang, S. Lin, O. S. Nakagawa, W. Xie, D. Sylvester, and C. Hu, "Effective on-chip inductance modeling for multiple signal lines and application on repeater insertion," *IEEE Transactions on VLSI Systems*, vol. 10, no. 6, pp. 799-805, December 2002.

[73] T. Sato, D. Sylvester, Y. Cao, and C. Hu, "Accurate in-situ measurement of peak noise and signal delay induced by interconnect coupling," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1587-1591, October 2001.

Conference Papers

[1] P.-Y. Chen, J. Seo, Y. Cao, S. Yu, "Compact oscillation neuron exploiting metal-insulator-transition for neuromorphic computing," *International Conference on Computer Aided Design*, a15.1-6, 2016.

[2] Y. Ma, N. Suda, J. Seo, Y. Cao, S. Vrudhula, "Scalable and modularized RTL compilation of convolutional neural networks onto FPGA," *International Conference on Field-Programmable Logic and Applications*, S5b.1-8, 2016.

[3] M. Tu, V. Berisha, Y. Cao, J. Seo, "Reducing the model order of deep neural networks using information theory," *IEEE Computer Society Annual Symposium on VLSI*, pp. 93-98, arXiv 1605.04859, 2016. **[invited]**

[4] S. Yin, Y. Ma, Y. Liu, C. Bae, S. Kim, S. Vrudhula, J. He, Y. Cao, J. Seo, "Low-power ECG biometric authentication for wearable systems featuring sparse memory compression," *ICML 2016 Workshop on On-device Intelligence*, pp. 1-5, 2016.

[5] A. Shrivastava, P. K. Deo, Z. Xu, P.-Y. Chen, S. Yu, Y. Cao, C. Chakrabarti, "Design of a reliable RRAM-based PUF for compact hardware security primitives," *International Symposium on Circuits and Systems*, pp. 2326-2329, 2016.

[6] A. Mohanty, N. Suda, M. Kim, S. Vrudhula, J. Seo, Y. Cao, "High-performance face detection with CPU-FPGA acceleration," *International Symposium on Circuits and Systems*, pp. 117-120, 2016. [**invited**]

[7] Z. Xu, P.-Y. Chen, J. Seo, S. Yu, Y. Cao, "Hardware-efficient learning with feedforward inhibition," International Nanoelectronics Conference, W5-1, pp. 1-2, 2016. **[invited]**

[8] M. Tu, V. Berisha, M. Woolf, J. Seo, Y. Cao, "Ranking the parameters of deep neural networks using the Fisher information," *International Conference on Acoustics, Speech and Signal Processing*, pp. 2647-2651, 2016.

[9] Y. Cao, S. Yu, Y. Wang, P.-Y. Chen, L. Xia, H. Yang, "Neuromorphic computing with resistive synaptic arrays: devices, circuits and systems," *International Symposium on Quality Electronic Design*, 2016. **[invited]**

[10] L. Xia, P.-Y. Chen, Y. Cao, S. Yu, Y. Wang, H. Yang, "MNSIM: Simulation platform for memristor-based neuromorphic computing system," *Design, Automation & Test in Europe*, pp. 469-474, 2016.

[11] N. Suda, V. Chandra, G. Dasika, A. Mohanty, Y. Ma, S. Vrudhula, J. Seo, Y. Cao, "Throughput-optimal OpenCL-based FPGA accelerator for large-scale convolutional neural networks," *International Symposium on Field-Programmable Gate Arrays*, pp. 16-25, 2016.

[12] S. Yu, P.-Y. Chen, Y. Cao, Y. Wang, H. Wu, "Scaling-up resistive synaptic arrays for neuro-inspired architecture: Challenges and prospect," *International Electron Devices Meeting*, pp. 451-454, 2015. **[invited]**

[13] Y. Ma, M. Kim, A. Mohanty, J. Seo, Y. Cao, S. Vrudhula, "Energy-efficient reconstruction of compressively sensed bioelectrical signals with stochastic computing circuits," *International Conference on Computer Design*, pp. 443-446, 2015.

[14] M. Mao, Y. Cao, S. Yu, C. Chakrabarti, "Optimizing latency, energy, and reliability of 1T1R ReRAM through appropriate voltage settings," *International Conference on Computer Design*, pp. 359-366, 2015.

[15] M. Mao, Y. Cao, S. Yu, C. Chakrabarti, "Programming strategies to improve energy efficiency and reliability of ReRAM memory systems," *IEEE Workshop on Signal Processing Systems*, pp. 1-6, 2015.

[16] P.-Y. Chen, B. Lin, I.-T. Wang, T.-H. Hou, J. Ye, J. Seo, S. Vrudhula, Y. Cao, S. Yu, "Mitigating effects of non-ideal synaptic device characteristics for on-chip learning," *International Conference on Computer Aided Design*, pp. 194-199, 2015.

[17] P.-Y. Chen, Y. Cao, C. Chakrabarti, S. Yu, "Exploiting resistive cross-point array for compact design of physical unclonable function," *IEEE Symposium on Hardware-Oriented Security and Trust*, pp. 26-31, 2015.

[18] R. Wang, Y. Cao, "Impact of temporal transistor variations on circuit reliability," *IEEE International Symposium on Circuits and Systems*, pp. 2453-2456, 2015. **[invited]**

[19] S. Yu, Y. Cao, "On-chip sparse learning with resistive cross-point array architecture," Great Lakes Symposium on VLSI, pp. 195-197, 2015. **[invited]**

[20] K. B. Sutaria, P. Ren, A. Mohanty, X. Feng, R. Wang, R. Huang, Y. Cao, "Duty cycle shift under static/dynamic aging in 28nm HK-MG technology," *International Reliability Physics Symposium*, CA.7.1-CA.7.5, 2015.

[21] K. B. Sutaria, X. Feng, P. Ren, R. Wang, R. Huang, Y. Cao, "Joint impact of PBTI and CHC on bias runaway at 28nm," *Government Microcircuit Applications & Critical Technology Conference*, pp. 24.1.1-24.1.4, 2015.

[22] P.-Y. Chen, D. Kadetotad, Z. Xu, A. Mohanty, B. Lin, J. Ye, S. Vrudhula, J. Seo, Y. Cao, S. Yu, "Technology-design co-optimization of resistive cross-point array for accelerating learning algorithms on chip," *Design, Automation & Test in Europe*, pp. 854-859, 2015.

[23] P. Gu, B. Li, T. Tang, S. Yu, Y. Wang, Y. Cao, "Technological exploration of RRAM crossbar array for matrix-vector multiplication," *Asia and South Pacific Design Automation Conference*, pp. 106-111, 2015.

[24] X. Feng, P. Ren, Z. Ji, R. Wang, K. B. Sutaria, Y. Cao, R. Huang, "Novel voltage step stress (VSS) technique for fast lifetime prediction of hot carrier degradation," *International Conference on Solid-State and Integrated Circuit Technology*, pp. 1-3, 2014.

[25] D. Kadetotad, Z. Xu, A. Mohanty, P.-Y. Chen, B. Lin, J. Ye, S. Vrudhula, S. Yu, Y. Cao, J. Seo, "Neurophysics-inspired parallel architecture with resistive crosspoint array for dictionary learning," *IEEE Biomedical Circuits and Systems Conference*, pp. 536-539, 2014.

[26] M. Mao, C. Yang, Z. Xu, Y. Cao, C. Chakrabarti, "Low cost ECC schemes for improving the reliability of DRAM+PRAM main memory," *IEEE Workshop on Signal Processing Systems*, pp. 1-6, 2014.

[27] Z. Xu, M. Cavaliere, P. An, S. Vrudhula, Y. Cao, "The stochastic loss of spikes in spiking neural P systems: Design and implementation of reliable arithmetic circuits," *The 12th Brainstorming Week on Membrane Computing*, pp. 353-373, 2014.

[28] K. B. Sutaria, A. Ramkumar, R. Zhu, Y. Cao, "Where is the Achilles heel under circuit aging," *IEEE Computer Society Annual Symposium on VLSI*, pp. 278-279, 2014. **[invited]**

[29] K. B. Sutaria, A. Ramkumar, R. Zhu, Y. Ma, Y. Cao, "BTI-induced aging under random stress waveforms: modeling, simulation and silicon validation," *Design Automation Conference*, pp. 1-6, 2014.

[30] K. B. Sutaria, P. Ren, X. Feng, A. Ramkumar, R. Zhu, R. Wang, R. Huang, Y. Cao, "Diagnosing bias runaway in analog/mixed signal circuits," *International Reliability Physics Symposium*, 2D.3.1-2D.3.6, 2014.

[31] M. Bajura, J. Ahlbin, I. S. Esqueda, S. Stansberry, P. Gadfort, M. Fritze, A. Ramkumar, K. Sutaria, Y. Cao, T.-F. Wu, C.-R. Ho, M. Chen, "Assessing long-term CMOS reliability for government IC applications," *Government Microcircuit Applications & Critical Technology Conference*, pp. 399-402, 2014.

[32] X. Chen, Y. Wang, Y. Cao, H. Yang, "Statistical analysis of random telegraph noise in digital circuits," *Asia and South Pacific Design Automation Conference*, pp. 161-166, 2014. **[best paper award nominee]**

[33] Z. Xu, K. B. Sutaria, C. Yang, C. Chakrabarti, Y. Cao, "Compact modeling of STT-MTJ for SPICE simulation," *European Solid-State Device Research & Circuits Conference*, pp. 338-341, 2013.

[34] M. Chen, V. Reddy, S. Krishnan, J. Ondrusek, and Y. Cao "ACE: A robust variability and aging sensor for high-k/metal gate SoC," *European Solid-State Device Research & Circuits Conference*, pp. 182-185, 2013.

[35] Y. Zhu, Y. Ye, Y. Cao, J. He, A. Zhang, H. He, H. Wang, C. Ma, Y. Hu, M. Chan, "Numerical study on effects of random dopant fluctuation in double gate tunneling FET," *IEEE Conference on Electron Devices and Solid-State Circuits*, pp. 1-2, June 2013.

[36] Y. Ye, Y. Zhu, H. He, J. Mei, Y. Cao, J. He, "Compact modeling of parameter variations of nanoscale CMOS due to random dopant fluctuation," *NSTI Nanotechnology Conference and Expo*, pp. 2:552-555, 2013.

[37] J. Velamala, K. Sutaria, H. Shimizu, H. Awano, T. Sato, G. Wirth, Y. Cao, "Logarithmic modeling of BTI under dynamic circuit operations: static, dynamic and long-term prediction," *International Reliability Physics Symposium*, CM.3.1-CM.3.5, 2013.

[38] J. Ahlbin, I. S. Esqueda, S. Stansberry, G. Boverman, M. Bajura, M. Fritze, C.-R. Ho, J. Hayong, L. Tian, N. Upadhyay, M. Chen, J. Velamala, K. Sutaria, V. Ravi, Y. Cao, "Techniques for estimating reliability for digital and analog CMOS circuits," *Government Microcircuit Applications & Critical Technology Conference*, 38-5.1-38-5.4, 2013.

[39] Z. Xu, K. Sutaria, C. Yang, C. Chakrabarti, Y. Cao, "SPICE modeling of STT-RAM for resilient design," *5th International MOS-AK/GSA Workshop*, 2012.

[40] Y. Emre, C. Yang, K. Sutaria, Y. Cao, C. Chakrabarti, "Enhancing the reliability of STT-RAM through circuit and system level techniques," *IEEE Workshop on Signal Processing Systems*, pp. 125-130, 2012.

[41] C. Yang, Y. Emre, Y. Cao, C. Chakrabarti, "Multi-tiered approach to improving the reliability of multi-level cell PRAM," *IEEE Workshop on Signal Processing Systems*, pp. 114-119, 2012.

[42] K. Sutaria, J. B. Velamala, Y. Cao, "Multi-level reliability simulation for IC design," *International Conference on Solid-State and Integrated Circuit Technology*, S07-03, pp. 1-4, 2012. **[invited]**

[43] Z. Xu, C. Yang, K. Sutaria, C. Chakrabarti, Y. Cao, "Hierarchical modeling of phase change memory for reliable design," *International Conference on Computer Design*, pp. 115-120, 2012.

[44] J. B. Velamala, K. Sutaria, H. Shimizu, H. Awano, T. Sato, Y. Cao, "Statistical aging under dynamic voltage scaling: a logarithmic model approach," *Custom Integrated Circuits Conference*, 6-3, pp. 1-4, 2012. **[best student paper nominee]**

[45] H. Luo, Y. Wang, Y. Cao, Y. Xie, H. Yang, "Temporal performance degradation under RTN: evaluation and mitigation for nanoscale circuits," *IEEE Computer Society Annual Symposium on VLSI*, pp. 183-188, 2012. **[best paper award]**

[46] S. Sinha, G. Yeric, B. Cline, V. Chandra, Y. Cao, "Design benchmarking to 7nm with FinFET predictive technology models," *International Symposium on Low Power Electronics and Design*, pp. 15-20, 2012.

[47] S. Sinha, G. Yeric, V. Chandra, B. Cline, Y. Cao, "Exploring sub-20nm FinFET design with predictive technology models," *Design Automation Conference*, pp. 283-288, 2012.

[48] J. Velamala, K. Sutaria, H. Shimuzu, T. Sato, Y. Cao, "Physics matters: statistical aging prediction under trapping/detrapping," *Design Automation Conference*, pp. 139-144, 2012. **[best paper award nominee]**

[49] S. Gummalla, A. Subramaniam, Y. Cao, C. Chakrabarti, "An analytical approach to efficient circuit variability analysis in scaled CMOS design," *International Symposium on Quality Electronic Design*, pp. 641-647, 2012.

[50] J. B. Velamala, K. B. Sutaria, T. Sato, Y. Cao, "Aging statistics based on trapping/detrapping: silicon evidence, modeling and long-term prediction," *International Reliability Physics Symposium*, 2F.2.1-2F.2.5, 2012.

[51] J. Velamala, V. Ravi, Y. Cao, "Failure diagnosis of asymmetric aging under NBTI," *International Conference on Computer Aided Design*, pp. 428-433, 2011.

[52] H. Luo, Y. Wang, J. Velamala, Y. Cao, Y. Xie, and H. Yang, "The impact of correlation between NBTI and TDDB on the performance of digital circuits," *International Midwest Symposium on Circuits and Systems*, pp. 1-4, 2011. **[invited]**

[53] S. Sinha, J. Suh, B. Bakkaloglu, Y. Cao, "A workload-aware neuromorphic controller for dynamic power and thermal management," *NASA/ESA Conference on Adaptive Hardware and Systems*, pp. 200-207, 2011.

[54] J. Velamala, R. LiVolsi, M. Torres, Y. Cao, "Design sensitivity of single event transients in scaled logic circuits," *Design Automation Conference*, pp. 694-699, 2011.

[55] R. Zheng, J. Suh, C. Xu, N. Hakim, B. Bakkaloglu, Y. Cao, "Programmable analog device array (PANDA): a platform for transistor-level analog reconfigurability," *Design Automation Conference*, pp. 322-327, 2011.

[56] H. Luo, X. Chen, J. Velamala, Y. Wang, Y. Cao, V. Chandra, Y. Ma, H. Yang, "Circuit-level delay modeling considering both TDDB and NBTI," *International Symposium on Quality Electronic Design*, pp. 14-21, 2011.

[57] M. Chen, V. Reddy, J. Carulli, S. Krishnan, V. Srinivasan, V. Rentala, and Y. Cao, "On-the-fly measurement of data path delay degradation in dynamic operations," *International Reliability Physics Symposium*, pp. 36-40, 2011.

[58] R. LiVolsi, K. McCornick, M. Torres, J. Velamala, R. Zheng, Y. Cao, "Correlation of no trouble found errors to negative temperature instability," *IEEE Aerospace Conference*, pp. 1-8, 10.1109/AERO.2011.5747585, 2011.

[59] Y. Cao, C.-C. Wang, Y. Ye, S. Gummalla, C. Chakrabarti, "Intrinsic variability in nano-CMOS design and beyond," *International Electron Devices Meeting*, pp. 414, 2010. **[invited]**

[60] W. Xu, S. Sinha, H. Wu, M. Dastagir, D. S. Gardner, Y. Cao, H. Yu, "Sub-100 μm scale on-chip inductors with CoZrTa for GHz applications," *The 55th Magnetism and Magnetic Materials Conference*, 2010.

[61] Y. Ye, C.-C. Wang. Y. Cao, "Simulation of random telegraph noise with 2-stage equivalent circuit," *International Conference on Computer Aided Design*, pp. 709-713, 2010.

[62] J. Sun, Y. Cao, J. Wang, "A self-evolving design methodology for power efficient multi-core systems," *International Conference on Computer Aided Design*, pp. 264-268, 2010.

[63] C.-Y. Chen, C.-C. Wang, Y. Ye, Y. Liu, J. Sato-Iwanaga, A. Inoue, H. Sorada, Y. Cao, R. W. Dutton, "A physics-based compact model for the 1/f noise in p-type Si/SiGe/Si heterostructure MOSFETs," *The Workshop on Synthesis and System Integration of Mixed Information Technologies*, R1-14, 2010.

[64] C.-C. Wang, Y. Ye, Y. Cao, "Compact modeling of Fe-FET and implications on variation-insensitive design," *International Conference on Simulation of Semiconductor Processes and Devices*, pp. 247-250, 2010.

[65] S. Sinha, J. Suh, B, Bakkaloglu, Y. Cao, "Workload-aware neuromorphic design of low-power supply voltage controller," *International Symposium on Low Power Electronics and Design*, pp. 241-246, 2010.

[66] J. Lee, C.-C. Wang, H. Gashami, L. Bircher, Y. Cao, and N. S. Kim, "Workload-adaptive process tuning strategy for power-efficient multi-core processors," *International Symposium on Low Power Electronics and Design*, pp. 225-230, 2010.

[67] S. Chellappa, J. Ni, X. Yao, N. Hindman, J. Velamala, M. Chen, Y. Cao, L. T. Clark, "In-situ characterization and extraction of SRAM variability," *Design Automation Conference*, pp. 711-716, 2010.

[68] J. B. Velamala, V. Reddy, R. Zheng, S. Krishnan, Y. Cao, "On the bias dependence of time exponent in NBTI and CHC effects," *International Reliability Physics Symposium*, pp. 650-654, 2010.

[69] E. Mintarno, R. Zheng, J. Velamala, Y. Cao, S. Boyd, R. W. Dutton, and S. Mitra, "Optimized self-tuning to maximize lifetime energy-efficiency in the presence of circuit aging," *Design, Automation and Test in Europe*, pp. 586-591, 2010.

[70] S. Nassif, N. Mehta, Y. Cao, "A resilience roadmap," *Design, Automation and Test in Europe*, pp. 1011-1016, 2010. **[invited]**

[71] C.-C. Wang, W. Zhao, F. Liu, M. Chen, Y. Cao, "Predictive modeling of layout-dependent stress effect in scaled CMOS design," *International Conference on Computer Aided Design*, pp. 513-520, 2009.

[72] S. Sinha, W. Xu, J. Velamala, M. Dastagir, B. Bakkaloglu, H. Yu, Y. Cao, "Enabling resonant clock distribution with scaled on-chip magnetic inductors," *International Conference on Computer Design*, pp. 103-108, 2009.

[73] R. Zheng, J. Velamala, V. Reddy, V. Balakrishnan, E. Mintarno, S. Mitra, S. Krishnan, Y. Cao, "Circuit aging prediction for low-power operation," *Custom Integrated Circuits Conference*, pp. 427-430, 2009.

[74] X. Li, W. Zhao, Y. Cao, Z. Zhu, J. Song, D. Bang, C.-C. Wang, S. H. Kang, J. Wang, M. Nowak, N. Yu, "Pathfinding for 22nm CMOS designs using predictive technology models," *Custom Integrated Circuits Conference*, pp. 227-230, 2009.

[75] C.-C. Wang, W. Zhao, M. Chen, Y. Cao, "Compact modeling of stress effects in scaled CMOS," *International Conference on Simulation of Semiconductor Processes and Devices*, pp. 1-4, 2009.

[76] X. Chen, Y. Wang, Y. Cao, Y. Ma, and H. Yang, "Variation-aware supply voltage assignment for minimizing circuit aging and leakage," *International Symposium on Low Power Electronics and Design*, pp. 39-44, 2009. **[best paper award nominee]**

[77] Y. Ye, F. Liu, M. Chen, Y. Cao, "Variability analysis under layout pattern-dependent rapid-thermal annealing process," *Design Automation Conference*, pp. 551-556, 2009.

[78] T.-B. Chan, V. Balakrishnan, Y. Cao, P. Gupta, "Extended burn-in for reduced V_{th} variation," *IEEE International Workshop on Design for Manufacturability and Yield (DFM&Y)*, pp. 25-28, 2009.

[79] Y. Wang, X. Chen, W. Wang, Y. Cao, Y. Xie, and H. Yang, "Gate replacement techniques for simultaneous leakage and aging optimization," *Design, Automation and Test in Europe*, pp. 328-333, 2009.

[80] Y. Wang, X. Chen, W. Wang, V. Balakrishnan, Y. Cao, Y. Xie, H. Yang, "On the efficacy of input vector control to mitigate circuit aging and leakage," *International Symposium on Quality Electronic Design*, pp. 19-26, 2009.

[81] Y. Cao, "What is Predictive Technology Model (PTM)?" ACM/SIGDA E-Newsletter, vol. 39, no. 3, March 2009. **[invited]**

[82] Y. Ye, F. Liu, Y. Cao, "Modeling of threshold voltage shift under pattern-dependent RTA process," *SPIE Design for Manufacturability through Design-Process Integration III*, vol. 7275, 72751T-1-9, 2009.

[83] C.-C. Wang, W. Zhao, F. Liu, M. Chen, Y. Cao, "Predictive modeling of layout-dependent stress effect in scaled CMOS design," *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, 2009.

[84] J. Ni, M. Chen, X. Lin, Y. Cao, "Adaptive transistor model for fast circuit simulation," *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, 2009.

[85] M. Debole, R. Krishnan, W. Wang, V. Balakrishnan, H. Luo, Y. Wang, Y. Cao, Y. Xie, V. Narayanan, "New-Age: A framework for NBTI estimation," *Asia and South Pacific Design Automation Conference*, pp. 455-460, 2009.

[86] C.-C. Wang, W. Zhao, Y. Cao, "Predictive modeling of layout-dependent carrier mobility in stressed CMOS technology," *SRC TECHCON*, 2008.

[87] V. Balakrishnan, W. Wang, Y. Cao, "Statistical prediction of circuit aging under process and design uncertainties," *SRC TECHCON*, 2008.

[88] W. Wang, V. Balakrishnan, B. Yang, Y. Cao, "Statistical prediction of NBTI-induced circuit aging," *International Conference on Solid-State and Integrated-Circuit Technology*, pp. 416-419, 2008. **[invited]**

[89] M. Agarwal, V. Balakrishnan, A. Bhuyan, K. Kim, B. C. Paul, W. Wang, Y. Cao, S. Mitra, "Optimized circuit failure prediction for aging: practicality and promise," *International Test Conference*, no. 26.1, 2008.

[90] W. Wang, V. Reddy, B. Yang, V. Balakrishnan, S. Krishnan, Y. Cao, "Statistical prediction of circuit aging under process variations," *Custom Integrated Circuits Conference*, pp. 13-16, 2008.

[91] Y. Ye, F. Liu, S. Nassif, Y. Cao, "Statistical modeling and simulation of threshold variation under dopant fluctuations and line-edge roughness," *Design Automation Conference*, pp. 900-905, 2008.

[92] S. Sinha, A. Balijepalli, Y. Cao, "A simplified model of carbon nanotube transistor with applications to analog and digital design," *International Symposium on Quality Electronic Design*, pp. 502-507, 2008.

[93] W. Wang, S. Yang, and Y. Cao, "Node criticality computation for circuit timing analysis and optimization under NBTI effect," *International Symposium on Quality Electronic Design*, pp. 763-768, 2008.

[94] X. Li, Y. Cao, "Projection-based piecewise-linear response surface modeling for strongly nonlinear VLSI performance variations," *International Symposium on Quality Electronic Design*, pp. 108-113, 2008.

[95] D. Ganesan, A. Mitev, J. Wang, Y. Cao, "Finite-point gate model for fast timing and power analysis," *International Symposium on Quality Electronic Design*, pp. 657-662, 2008.

[96] L. Cheng, Y. Lin, L. He, and Y. Cao, "Trace-based framework for concurrent development of process and FPGA architecture considering process variation and reliability," *International Symposium on Field-Programmable Gate Arrays*, pp. 159-168, 2008.

[97] Y. Ye, F. Liu, S. Nassif, Y. Cao, "Statistical modeling and simulation of threshold voltage variation under dopant fluctuations and line-edge roughness," *9th Annual Austin CAS Conference*, 2008.

[98] M. Agarwal, V. Balakrishnan, A. Bhuyan, K. Kim, M. Mizuno, B. C. Paul, W. Wang, Y. Cao, S. Mitra, "Optimized circuit failure prediction for aging: practicality and promise," *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, 2008.

[99] A. Subramaniam, R. Singal, C.-C. Wang, Y. Cao, "Design rule optimization of regular layout for leakage reduction in nanoscale design," *Asia and South Pacific Design Automation Conference*, pp. 474-479, 2008.

[100] W. Zhao, X. Li, M. Nowak, and Y. Cao, "Predictive technology modeling for 32nm low power design," *International Semiconductor Device Research Symposium*, TA4-03, 2007.

[101] W. Wang, Z. Wei, S. Yang, Y. Cao, "An efficient method to identify critical gates under circuit aging," *International Conference on Computer Aided Design*, pp. 735-740, 2007.

[102] D. Ganesan, D. Shanmugasundaram, A. Mitev, Y. Cao, J. Wang, "A robust finite-point based gate model considering process variations," *International Conference on Computer Aided Design*, pp. 692-697, 2007.

[103] Y. Cao, C. C. McAndrew, "MOSFET modeling for 45nm and beyond," embedded tutorial, *International Conference on Computer Aided Design*, pp. 638-643, 2007. **[invited]**

[104] W. Wang, V. Reddy, A. T. Krishnan, S. Krishnan, Y. Cao, "An integrated modeling paradigm of circuit reliability for 65nm CMOS technology," *Custom Integrated Circuits Conference*, pp. 511-514, 2007.

[105] W. Zhao, F. Liu, K. Agarwal, D. Acharyya, S. Nassif, K. Nowka, Y. Cao, "Rigorous extraction of process variations for 65nm CMOS design," *European Solid-State Circuits Conference*, pp. 89-92, 2007.

[106] W. Wang, V. Reddy, A. T. Krishnan, S. Krishnan, Y. Cao, "An integrated modeling paradigm of circuit reliability for 65nm CMOS technology," *SRC TECHNON*, 2007.

[107] A. Balijepalli, S. Sinha, Y. Cao, "Compact modeling of carbon nanotube transistor for early stage process-design exploration," *International Symposium on Low Power Electronics and Design*, pp. 2-7, 2007. **[best paper award]**

[108] W. Wang, S. Yang, S. Bhardwaj, R. Vattikonda, F. Liu, S. Vrudhula, Y. Cao, "The impact of NBTI on the performance of combinational and sequential circuits," *Design Automation Conference*, pp. 364-369, 2007.

[109] R. Singal, A. Balijepalli, A. Subramaniam, F. Liu, S. Nassif, Y. Cao, "Modeling and analysis of non-rectangular gate for post-lithography circuit simulation," *Design Automation Conference*, pp. 823-828, 2007.

[110] M. Chen, W. Zhao, F. Liu, Y. Cao, "Fast statistical circuit analysis with finite-point based transistor model," *Design, Automation and Test in Europe*, pp. 1391-1396, 2007.

[111] A. Balijepalli, J. Ervin, Y. Cao, and T. Thornton, "Compact modeling of a PD SOI MESFET for wide-temperature designs," *International Symposium on Quality Electronic Design*, pp. 133-138, 2007.

[112] R. Vattikonda, Y. Luo, A. Gyure, X. Qi, S. Lo, M. Shahram, Y. Cao, K. Singhal, and D. Toffolon, "A new simulation method for NBTI analysis in SPICE environment," *International Symposium on Quality Electronic Design*, pp. 41-46, 2007.

[113] T. Sairam, W. Zhao, Y. Cao, "Optimizing FinFET technology for high-speed and low-power design," *Great Lakes Symposium on VLSI*, pp. 73-77, 2007. **[best paper award nominee]**

[114] W. Zhao, F. Liu, K. Agarwal, D. Acharyya, S. Nassif, K. Nowka, Y. Cao, "Extraction and modeling of process variations for robust nanoscale design," *8th Annual Austin CAS Conference*, 2008.

[115] B. T. Cline, K. Chopra, D. Blaauw, and Y. Cao "Analysis and modeling of CD variation for statistical static timing," *International Conference on Computer Aided Design*, pp. 60-66, 2006.

[116] Y. Cao, W. Zhao, "Predictive technology model for nano-CMOS design exploration," *International Conference on Nano-Networks*, 2006. **[invited]**

[117] S. Bhardwaj, W. Wang, R. Vattikonda, Y. Cao, S. Vrudhula, "Predictive modeling of the NBTI effect for reliable design," *Custom Integrated Circuits Conference*, pp. 189-192, 2006.

[118] R. Vattikonda, W. Wang, Y. Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," *Design Automation Conference*, pp. 1047-1052, 2006.

[119] S. Bhardwaj, S. Vrudhula, Praveen Ghanta, Y. Cao, "Modeling of intra-die process variations for accurate analysis and optimization of nanoscale circuits," *Design Automation Conference*, pp. 791-796, 2006.

[120] A. Balijepalli, J. Ervin, P. Joshi, J. Yang, Y. Cao, and T. J. Thornton, "High-voltage CMOS compatible SOI MESFET characterization and SPICE model extraction," *IEEE International Microwave Symposium*, pp. 1335-1338, 2006.

[121] S. Bhardwaj, S. Vrudhula, and Y. Cao, "LOTUS: leakage optimization under timing uncertainty for standard-cell designs," *International Symposium on Quality electronic Design*, pp. 717-722, 2006.

[122] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45nm design exploration," *International Symposium on Quality Electronic Design*, pp. 585-590, 2006. **[best paper award nominee]**

[123] M. Chen and Y. Cao, "Analysis of pulse signaling for low-power on-chip global bus design," *International Symposium on Quality electronic Design*, pp. 401-406, 2006.

[124] S. Bhardwaj, Y. Cao, and S. Vrudhula, "Statistical leakage minimization using gate sizing, gate length biasing and threshold voltage selection," *Asia and South Pacific Design Automation Conference*, pp. 953-958, 2006. **[best paper award nominee]**

[125] J. Chen, L. T. Clark, Y. Cao, "Robust subthreshold design of high fan-in/out circuits," *International Conference on Computer Design*, pp. 405-410, 2005.

[126] Y. Cao and L. T. Clark, "Mapping statistical process variations toward circuit performance variability: an analytical modeling approach," *Design Automation Conference*, pp. 658-663, 2005.

[127] P. Friedberg, Y. Cao, J. Cain, R. Wang, J. Rabaey, and C. Spanos, "Modeling within-die spatial correlation effects for process-design co-optimization," *Microlithography Program, SPIE*, 2005.

[128] P. Friedberg, Y. Cao, J. Cain, R. Wang, J. Rabaey, and C. Spanos, "Modeling within-die spatial correlation effects for process-design co-optimization," *International Symposium on Quality Electronic Design*, pp. 516-521, 2005.

[129] Z. Wei, Y. Cao, and R. Newton, "Digital image restoration by exposure-splitting and registration," *International Conference on Pattern Recognition*, vol. 4, pp. 23-26, 2004.

[130] A. Vladimirescu, Y. Cao, O. Thomas, H. Qin, D. Markovic, A. Valentian, R. Ionita, J. Rabaey, A. Amara, "Ultra-low-voltage robust design issues in deep-submicron CMOS," *IEEE Northeast Workshop on Circuits and Systems*, pp. 49-52, 2004. **[invited]**

[131] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu, and J. Rabaey, "SRAM leakage suppression by minimizing standby supply voltage," *International Symposium on Quality Electronic Design*, pp. 55-60, 2004. **[best paper award]**

[132] Y. Cao, H. Qin, R. Wang, P. Friedberg, A. Vladimirescu, and J. Rabaey, "Yield optimization with energy-delay constraints in low-power digital circuits," *IEEE Conference on Electron Devices and Solid-State Circuits*, pp. 285-288, Dec. 2003.

[133] R. Chang, Y. Cao, and C. Spanos, "Modeling metal dishing for interconnect optimization," *IEEE International Electron Devices Meeting*, pp. 249-252, Dec. 2003.

[134] Y. Cao, X. Yang, X. Huang, and D. Sylvester, "Switching-factor based loop RLC modeling for efficient timing analysis," *International Conference on Computer Aided Design*, pp. 848-853, Nov. 2003.

[135] A. M. Niknejad, M. Chan, C. Hu, B. Brodersen, J. Xi, J. He, S. Emami, C. Doan, Y. Cao, P. Su, H. Wan, M. Dunga, C. H. Lin, "Compact modeling for RF and microwave integrated circuits," *Proceedings of Nanotech Conference*, vol. 2., pp. 294-297, February 2003. **[invited]**

[136] Y. Cao, X. Huang, D. Sylvester, T. King, and C. Hu, "Impact of frequency-dependent interconnect impedance on digital and RF design," *IEEE International ASIC/SoC Conference*, pp. 438-442, Sep. 2002.

[137] Y. Cao, P. Gupta, C. Hu, A. B. Kahng, D. Sylvester, and J. Yang, "Design sensitivities to variability: extrapolations and assessments in nanometer VLSI," *IEEE International ASIC/SoC Conference*, pp. 411-415, Sep. 2002.

[138] X. Huang, Y. Cao, D. Sylvester, T. King, and C. Hu, "Analytical performance models for RLC interconnects and applications to clock optimization," *IEEE International ASIC/SoC Conference*, pp. 353-357, Sep. 2002.

[139] Y. Cao, R. A. Groves, N. D. Zamdmer, J. Plouchart, R. A. Wachnik, X. Huang, T. King, and C. Hu, "Frequency-independent equivalent circuit model for on-chip spiral inductors," *Proceedings of Custom Integrated Circuits Conference*, pp. 217-220, Jun. 2002.

[140] X. Huang, P. Restle, T. Bucelot, Y. Cao, and T. King, "Loop-based interconnect modeling and optimization approach for multi-GHz clock network design," *Proceedings of Custom Integrated Circuits Conference*, pp. 19-22, Jun. 2002.

[141] K. Agarwal, Y. Cao, T. Sato, D. Sylvester, and C. Hu, "Efficient generation of delay change curves for noise-aware static timing analysis," *Proceedings of Asia and South Pacific Design Automation Conference*, pp. 77-84, Jan. 2002.

[142] Y. Cao, X. Huang, N. Chang, S. Lin, S. Nakagawa, W. Xie, and C. Hu, "Effective on-chip inductance modeling for multiple signal lines and application on repeater insertion," *Proceedings of International Symposium on Quality Electronic Design*, pp. 185-190, Sep. 2001.

[143] Y. Cao, X. Huang, D. Sylvester, N. Chang, and C. Hu, "A new analytical delay and noise model for on-chip RLC interconnect," *Technical Digest of International Electron Devices Meeting*, pp. 823-826, Dec. 2000.

[144] X. Huang, Y. Cao, D. Sylvester, S. Lin, T. King, and C. Hu, "RLC signal integrity analysis of high-speed global interconnect," *Technical Digest of International Electron Devices Meeting*, pp. 731-734, Dec. 2000.

[145] Y. Cao, T. Sato, X. Huang, C. Hu, and D. Sylvester, "New approaches to noise-aware static timing analysis," *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, pp. 8-13, Dec. 2000.

[146] Y. Cao, C. Hu, X. Huang, A. B. Kahng, S. Muddu, D. Stroobandt, D. Sylvester, "Effects of global interconnect optimizations on performance estimation of deep submicron designs," *Proceedings of International Conference on Computer Aided Design*, pp. 56-61, Nov. 2000.

[147] T. Sato, Y. Cao, D. Sylvester, and C. Hu, "Characterization of interconnect coupling noise using in-situ delay change curve measurements," *Proceedings of IEEE ASIC/SoC Conference*, pp.321-325, Sep. 2000.

[148] Cardwell, Y. Cao, A. B. Kahng, F. Koushanfar, L. Hua, I. L. Markov, M. Oliver, D. Stroobandt, D. Sylvester, "GTX: the MARCO GSRC technology extrapolation system," *Proceedings of Design Automation Conference*, pp. 693-698, Jun. 2000.

[149] Y. Cao, T. Sato, D. Sylvester, M. Orshansky, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit design," *Proceedings of Custom Integrated Circuits Conference*, pp. 201-204, Jun. 2000.

[150] T. Sato, D. Sylvester, Y. Cao, and C. Hu, "Accurate in-situ measurement of peak noise and signal delay induced by interconnect coupling," *IEEE International Solid-State Circuits Conference*, pp. 226-227, Feb. 2000. **[Beatrice winner award]**