Curriculum Vitæ

Sarma Vrudhula
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Biography

Sarma Vrudhula (Website) is a Professor in the School of Computing and Augmented Intelligence at Arizona State University, Tempe AZ, and the Director of the NSF IUCRC Center for Embedded Systems (https://ces.asu.edu). His areas of research and teaching are mostly centered around VLSI design and Computer-Aided Design and Design Automation for VLSI, focusing on low power design and energy management of circuits and systems. His active areas of research include:

- system level dynamic power and thermal management of multicore processors and system-on-chip (SoC)
- energy efficient edge computing
- design of energy-efficient ASIC and FPGA implementations of neural networks
- new approaches to logic design with spintronic devices, RRAMs and flash transistors
- low power, non-volatile logic
- energy optimization of battery powered computing systems
- statistical methods for the analysis of process variations
- statistical optimization of performance, power and leakage
- digital implementation of perceptrons for power, performance and area optimization of ASICs and FPGAs

In these areas he has authored or co-authored more than 230 papers in journals and conferences, and holds 17 patents, 16 of which are joinlty with his students. In addition to research and teaching, he has led several teams. In 1996 he established the NSF Center for Low Power Electronics (CLPE) at the University of Arizona, in collaboration with the EE department of the Arizona State University. CLPE was supported by the NSF, the State of Arizona, and many leading companies in the microelectronics industry. Through CLPE, he has facilitated the research of twenty faculty and over 40 graduate students across both campuses. He is also the founding director of the NSF I/UCRC Center for Embedded Systems at ASU.

Recognitions: He was made Fellow of the IEEE in 2016 for "*contributions to low power and energy-efficient design of digital circuits and systems.*", and elected as member of National Academy of Inventors in 2017. He has received three best paper awards (2017, 2016, 2008), an outstanding paper award (2001) and a best researcher (CS department internal) award (2011).

He received the B.Math (Honors) from the University of Waterloo, Ontario, Canada, and the M.S. and Ph.D degrees in electrical engineering from the University of Southern California. Prior to joining ASU, he was on the faculty of the EE-Systems department of the University of Southern California and professor in the Electrical and Computer Engineering department at the University of Arizona, in Tucson, AZ.

Education

B.Math Mathematics and Computer Science, 1976
University of Waterloo, Waterloo, Canada.

M.S. Electrical Engineering, 1981
University of Southern California, Los Angeles.

Ph.D. Electrical Engineering, 1985
University of Southern California, Los Angeles.

Employment

Feb. '09 - Present	Director, NSF IUCRC Center for Embedded Systems
Jan. '05 - Present	Professor, School of Computing and Augmented Intelligence., Arizona State University, Tempe AZ.
Apr. '96 - Dec. '04	Director, NSF S/IUCRC Center for Low Power Electronics University of Arizona, Tucson, AZ.
Apr. '96 - Dec. '04	Professor, Electrical and Computer Engineering Dept. University of Arizona, Tucson, AZ
Aug. '92 - July '96	Associate Professor, Electrical and Computer Engineering Dept. University of Arizona, Tucson, AZ
Jan. '85 - Aug. '92	Assistant Professor, Dept. of Electrical Enginering-Systems University of Southern California, Los Angeles, CA.
Sept. '81 - Dec. '84	Research Assistant, Dept. of Electrical Enginering-Systems University of Southern California, Los Angeles, CA.
Apr. '82 - Sept. '82	Member of Technical Staff, IBM, Hopewell Junction, NY.
June '78 - Sept. '81	Member of Research Staff, USC Information Sciences Institute Marina Del Rey, CA.
Sept. '76 - Sept. '77	Member of Technical Staff, Bell Canada, Toronto, Canada.

- Elected Senior member of *National Academy of Inventors*, 2020.
- *Best Paper Award:* "*Statistical Library Characterization Using Arbitrary Polynomial Chaos*", Mehmet Ince, Sule Ozev and Sarma Vrudhula, 8th Latin American Symposium on Circuits and Systems, Bariloche, Argentina, March 2017.
- *IEEE Fellow*, for "*contributions to low power and energy-efficient design of digital circuits and systems*", 2016.
- *Best Paper Award:* "*Digital IP Protection Using Threshold Voltage Control*", with Joseph Davis, Niranjan Kulkarni,Jinghua Yang, Aykut Dengi. International Symposium of Quality Electronic Design (ISQED), 2016.
- *Best Researcher:* (Senior Faculty), School of Computing, Informatics and Decision Systems Engineering, ASU, 2011.
- *Outstanding Researcher:* School of Computing, Informatics and Decision Systems Engineering, ASU, 2010.
- *Best Paper Award:* "A methodology for characterization of large macro cells and IP blocks considering process variations", with Amit Goel, Feroze Taraporevala, Praveen Ghanta. International Symposium of Quality Electronic Design (ISQED), 2008.
- *Outstanding Paper Award:* for "Performance Driven Placement and Routing for Field Programmable Analog Arrays", with Haibo Wang and Olek Palusinski. International Conference on Mixed Design of Integrated Circuits and Systems, Zakopane, Poland, 2001.
- *Distinguished Scientist*, Silesian University of Technology, Gliwice, Poland, and University of Mining and Metallurgy, Akademia Gorniczo-Hutnicza, 2000, 2001.

Journals and Book Chapters

[86] Ankit Wagle, Jinghua Yang, Niranjan Kulkarni, and Sarma Vrudhula. A New Approach to Clock Skewing for Area and Power Optimization of ASICs using Differential Flipflops and Local Clocking. *IEEE Transactions on Computer-Aided Design of VLSI Systems (TCAD)*, Accepted 2023.

[85] Sunil P. Khatri, Sarma Vrudhula, Monther Abusultan, Kunal Bharathi, Shao-Wei Chu, Cheng-Yen Lee, Kyler R. Scott, Gian Singh, and Ankit Wagle. *Flash: A "Forgotten" Technology in VLSI Design*, pages 67–136. Springer International Publishing, 2023.

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[83] Ankit Wagle, Gian Singh, Sunil Khatri, and Sarma Vrudhula. A Novel ASIC Design Flow using Weight-Tunable Binary Neurons as Standard Cells. *IEEE Transactions on Circuits and Systems (TCAS)*, 69(7), Jul. 2022. doi: 10.1109/TCSI.2022.3164995.

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[81] Mehdi Ghasemi, Daler Rakhmatov, Carole-Jean Wu, and Sarma Vrudhula. EdgeWise: Energy-Efficient CNN Computation on EdgeDevices under Stochastic Communication Delays. *ACM Transactions on Embedded Systems (ACMTECS)*, Apr. 2022.

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Conferences

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- *Analysis of Leakage and Timing in the presence of process variations*, LSI Logic Inc., Aug. 30, 2007.
- *Robust design of nano-scale circuits in the presence of process variations*, Full-day tutorial given at the IEEE International Conference on VLSI Design, Bangalore, India, Jan 7, 2007.
- *Stochastic Analysis of interconnects and power grids in the presence of process variations*, First International Workshop on Interconnect Design and Variability, Bangalore, India, Dec. 28-29, 2006.
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- *Energy Management in Battery Powered Embedded Systems*, EECS Dept., University of Michigan, Ann Arbor, MI Mar. 2004.
- *Analysis and Optimization of Power and Performance of Digital Circuits and Systems*, ST Microelectronics, Phoenix, AZ, Feb. 2004.

- *Statistical Approach to Signal Integrity and Performance Analysis of DSM CMOS Circuits*, Connection One, Arizona State University, Jan. 2004.
- *Battery-Aware Design of Portable Embedded Systems*, **Distinguished Speaker**, Embedded Systems Research Center (ESRC), Seoul National University, Aug. 28, 2003.
- *Identification of the Minimum Leakage States*, Cadence Inc., San Jose CA, Oct. 2003.
- *Statistical Gate Sizing to Improve Timing Yield*
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- *Approaches to Minimizing Subthreshold Leakage*, Mindspeed Inc., Irvine CA, June 2003.
- *Energy Management in Battery Powered Embedded Systems*, IBM ARL, Austin, TX, June 2003.
- *Probabilistic Analysis of Interconnect Coupling Noise in Deep Submicron Circuits*
  - **Distinguished Speaker**, Silesian University of Technology, Gliwice, Poland, June 2001.
  - **Distinguished Speaker**, University of Mining and Metallurgy, Akademia Gorniczo-Hutnicza, June 2001.
  - Motorola Inc., Austin TX, Aug. 2001.
  - Center for Low Power Electronics (nationally broadcast), Oct. 2001.
- *Algorithms for Minimizing Standby Power in Dual VT CMOS Circuits*
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6. Elham Azari, *Reduced Order Models and Approximations for Hardware Acceleration of Neural Networks*, Ph.D. Computer Engineering, 2021.
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16. Vinay Hanumaiah *Unified Framework for Energy-Proportional Computing in Multicore Processors: Novel Algorithms and Practical Implementation*, Ph.D, Electrical Engineering, 2013.
17. Yang Hu, *Testing of threshold logic latch based hybrid circuits*, MS, Electrical Engineering, 2013.
18. Benjamin Gaudette, *Energy Management in Solar Powered Wireless Sensor Networks*, MS Computer Science, 2012.
19. Tejaswi Lingegowda, *Threshold Logic Properties and Methods: Applications to post-CMOS Design Automation and Gene Regulation Modeling*, Ph.D. 2011

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23. Amit Goel, *Characterization of nanoscale digital circuits for statisical timing and signal integrity analysis*, MSEE 2008.

24. Ravishankar Rao, *Fast and accurate techniques for early design space exploration and dynamic thermal management of multi-core processors*, Ph.D. Electrical Engineering, 2008.

25. Sudheendra Kadri, *Performance driven design space exploration in portable devices powered by fuel cell battery hybrid system*, MSEE 2007.

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29. Sreeja Raj, *Statistical Timing Analysis*, MSEE 2004.

30. Sridhar Dasika, *Energy Management of Sensor Networks*, MSEE 2004.

31. Kaviraj Chopra, *Symbolic Algorithms for Identifying Minimum and Bounded Leakage States*, MSEE 2004.

32. Raghukiran Sreeramaneni, *Energy Profiler for Hardware-Software Codesign*, MSEE 2003.

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35. Haibo Wang, *Field Programmable Analog Array Synthesis*, Ph.D. 2002.

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37. Daler Rakhmatov, *Dynamic Scheduling in Runtime Reconfigurable Systems*, MSEE 1998.

38. Yukti Bareja, *RTL Level Power Estimation*, MSEE 1998.

39. Thomas J. Brown, *Algorithms for Clustering of Dataflow Graphs for Implementation on Dynamically Configurable FPGAs*, MSEE 1998.

40. David Rutishauser, *Object Oriented Simulation of a GPS Receiver*, MSEE 1998.

41. Bryce A. Rasmussen, *A Design of a Counterflow Pipeline Processor*, MSEE 1997.
42. Kendel McCarley, *Design of an High Performance Asynchronous Floating Point Unit*, MSEE 1996.
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45. Hong-Yu Xie, *Gate Level Power Estimation*, MSEE 1995.
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Arizona State University:

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- Director Search Committee, School of Computing and Augmented Intelligence, 2022.
- Panelist, Faculty Women's Association, Promotion and Tenure, 2022.
- Targeted faculty recruitment for SCAI, 2021.
- Fulton Schools of Engineering Dean's Faculty Advisory Committee, 2020-2023.
- University Tenure and Promotion Committee, 2016-2019.
- Search Committee for Director of CIDSE, 2016-2017.
- Undergraduate Program Committee for CSE, 2014-2014, 2015-2016, 2016-2017, 2020-2022, 2022-2024.
- Graduate Program Committee for CENG, 2013-2014, 2014-2015, 2015-2016, 2016-2017.
- Search Committee for Dean of Fulton School of Engineering, 2015-2016.
- Chair, Faculty Recruiting Committee, *Next Generation Computing*, 2012-2013, 2013-2014, 2014-2015.
- Director of Research, Consortium for Embedded Systems, 2005 -
- Chair, Computer Engineering Program Committee, Fulton School of Engineering, 2009.
- Graduate Program Committee, Committee, Computer Science and Engineering, 2008-2010.
- Personnel Committee, Computer Science and Engineering, 2005-2007.
- Chair, Faculty Recruiting Committee, Committee, Computer Science and Engineering, 2005.
- Academic Senate, Arizona State University, 2005-2006.

University of Arizona:

- Promotion & Tenure Committee, Electrical and Computer Engineering Department, 2002-2004.
- Director Summer Internship Program (SPIN) for CLPE, 1996-2004.
- Chair, Faculty Recruiting Committee, Electrical and Computer Engineering Dept., 1997-1998, 2000-2003.
- Computer Engineering Faculty Recruiting Subcommittee, 1993-1994, 1996.

- Undergraduate Curriculum Committee, Electrical and Computer Engineering Dept., 1996-1997.
- Graduate Student Recruiting and Awards Committee, Electrical and Computer Engineering Dept.
- Computer Engineering Curriculum, Electrical and Computer Engineering Dept., 1992-1993, 1996-1997.
- Peer Evaluation Committee, Electrical and Computer Engineering Dept., 1995-1997.
- Chair, Computer Policy Committee, Electrical and Computer Engineering Dept., 1993-1996.
- International Graduate Admissions, Electrical and Computer Engineering Dept., 1994-1996.

Journal Editorships, Program and Other Commitees

- IEEE Fellow Committee, 2022
- Track Chair, IEEE/ACM International Conference on Computer-Aided Design, 2022.
- Associate Editor *IEEE Transactions on Sustainable Computing*, 2020.
- IEEE Fellow Committee, 2017.
- Invited Nominator for the Kyoto Prize, 2016.
- Associate Editor *IEEE Transactions on Multi-Scale Computing Systems (TMSCS), 2015-2016.*
- Associate Editor *IEEE Transactions on Computer-Aided Design* (TCAD), 2006-2013.
- Associate Editor *ACM Transactions on Design Automation of Electronic Systems* (TODAES), 2006-2009.
- Associate Editor *IEEE Transactions on VLSI Systems*, 1996-1998.
- Member of Editorial Board, *Studia Informatica*, Silesian University of Technology Press, Gliwice, Poland, 2001-2002.
- Member of the Board of Directors: Computer Systems Support Solutions, 1998.
- External Reviewer, Computer Engineering Program, Southern Illinois University, Carbondale, 2002.
- Program Committee Member:
  - *Symposium on Biomorphic Circuits & Systems with Threshold Logic*, (BioTL) 2014.
  - *IEEE/ACM International Symposium on Nanoscale Architectures* (NANOARCH), 2014.
  - *IEEE International Symposium on Low Power Electronic Design* (ISLPED), 2014.
  - *IEEE International Conference on Computer Aided Design* (ICCAD), 2014.
  - *IEEE International Conference on Computer Aided Design* (ICCAD), 2013.
  - *IEEE/ACM Design Automation Conference*, 2001-2004, 2014.
  - *IEEE International Conf on Embedded Software and Systems*, China. 2005.
  - *International. Symposium on Quality Electronic Design* (ISQED), 2003-2006.
  - *Mixed Design of Integrated Circuits and Systems*, Poland, 2000-2001.
  - *Southwest Symposium on Mixed-Signal Design*, 1999.
  - *International Conference on Computer Design* (ICCD), 1993-1997.
  - *NSF S/IUCRC Symposium at the University of Oklahoma*, 1997.
- Chair, Vice-Chair, Organizer Positions:

- *Organizer* of Special Session on “”Toward On-Chip Cortical Computng”, IEEE/ACM Design Automation Conference (DAC), Sanfrancisco, CA, June 2014.
- *Organizer* of Special Session on “”Neuron Inspired Computing using Nanotechology”, 9th Asia and South Pacific Design Automation Conference (ASP-DAC), Singapore, 2014.
- *Chair* Technical Program Comittee (RDIC), *International. Symposium on Quality Electronic Design* (ISQED), 2005-2006.
- *Chair* Technical Program Committee (Power), IEEE/ACM Design Automation Conference, 2005-2006.
- *Organizer* and *Chair* of Special Session on “Error Tolerant Design”, IEEE/ACM Design Automation Conference, 2005.
- *Session Chair*, Sensor Networks and Communication Systems, International. Symposium on Low Power Electronic Design (ISLPED), Seoul, Korea, 2003.
- *Chair, National Science Foundation S/IUCRC Symposium*, 1999.
- *Vice Chair, IFIP Working Group on Hardware/Software co-Design*, 1998.
- *Track Chair, IEEE International. Conference on Computer Design (ICCD)*, 1998.
- *Organizer and Session Chair on Dynamically Reconfigurable Architectures*, IEEE International. Conference on Computer Design (ICCD), 1998.
- *VLSI/VHSIC Session Chair, Phoenix Conference on Computers and Communications*, 1993.
- General Chairman of *Second International Workshop on The Economics of Design and Test*, 1993.

- Reviewing and Refereeing
  - Invited External Reviewer for the Portuguese National Science Foundation
  - IEEE International Conference on Computer Design
  - IEEE International Conference on Computer-Aided Design
  - IEEE International Conference on Computers and Communications
  - IEEE VLSI Test Symposium
  - IEEE Design Automation Conference
  - Journal of Electronic Testing and Test Applications
  - ACM Transactions on Design Automation
  - IEEE Transactions on VLSI Systems
  - IEEE Transactions on CAD
  - Journal of Integrated Computer-Aided Engineering
  - IEE Proceedings
  - Proposals for the National Science Foundation