**DOUGLAS ALAN GARRITY**
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EDUCATION: BSEE Portland State University, Portland, Oregon
Graduation Date: June 1986

MSEE University of Idaho, Moscow, Idaho
Graduation Date: May 1993

Ph. D. Electrical Engineering Arizona State University, Tempe, Arizona
Graduation Date: December 2007

EMPLOYMENT: *May 2009 to present:* (named a Freescale Fellow in October 2010 (1 of 12 out of 21,000 employees) ) Director of Freescale Data Converter Center of Excellence (DCCOE), Freescale Semiconductor, Inc. 2100 E. Elliot Road, Tempe AZ 85284.
Responsible for data converter development and data converter IP for entire corporation. Worked with DCCOE to develop 24-bit analog front end for electricity metering. Also worked with DCCOE team to develop ultra-low cost high-performance $\Sigma\Delta$ ADC for automotive applications and continuous-time $\Sigma\Delta$ ADC for various radio receivers as well as ADCs for automotive radar receivers.

*Mar. 1992 to April 2009:* Analog Design (R&D) Engineer, Freescale Semiconductor, Inc./Motorola Inc.,
2100 East Elliot Road, Tempe AZ 85284.
Responsible for research into advanced data converter design techniques and new process capabilities for low power and/or high performance applications including LTE, DVB, Set-Top Box, Cellular, Automotive, etc. Managed team of fourteen research engineers in this effort.

Fall Semester 2008, 2011, 2012: Adjunct Professor, Arizona State University (ASU), Tempe, Arizona.
Developed (from previous versions of course material) and taught a graduate-level (EEE 627) course on Oversampled Noise-Shaping ($\Sigma\Delta$) Analog-to-Digital Converters (ADCs).

Spring Semester 2009,2012: Adjunct Professor, Arizona State University (ASU), Tempe, Arizona.
In the process of developing (from previous versions of course material) and teaching a graduate-level (EEE 527) course on Nyquist-Rate ADCs.

Developed and patented a single ADC that samples two channels (I and Q) in a broadband radio receiver. The ADC architecture includes a number of innovations including a multi-phase non-overlapping clock generator and a multi-input delaying/holding switch-capacitor gain stage. A paper describing this work was published in the June 2008 issue of the IEEE Journal of Solid-State Circuits.

Developed and patented multiple ultra-low power analog-to-digital converter architectures for use in portable applications. A 10 bit version of one of the ADC that samples at 1MHz, dissipates 1.3mW and occupies $0.085mm^2$. ADCs based on this architecture have been designed into nearly every cell phone and/or radio that Motorola sells.

Lead research team in the design and development of a bandpass $\Sigma-\Delta$ Analog to Digital Converter for use in a portable radio.

Completed the design of a10 bit 40Msps very low power BiCMOS pipelined ADC. This architecture has also been used extensively in Motorola products.

Completed the design of a low glitch energy current switch for use in a high speed, high resolution current output DAC. Also participated in the system design and the design of various blocks for a high speed, high resolution ADC.

Completed the following ADC designs that operate from a 2.7V supply: a 10 bit 2Msps cyclic ADC that dissipates <15mW, and a 10 bit 20Msps pipelined ADC that dissipates <80mW. A paper on the cyclic ADC has been presented at the 1996 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) in September 1996.

Designed Fully Differential Switched Capacitor Filters for a cordless phone I.C. with 1.8V supply voltage operation.

Conducted extensive research into subthreshold operation of MOS transistors and designed a constant current source based on this research. A paper was also written and presented at a Motorola internal conference as mentioned below.

*Oct. 1989 to Mar. 1992:* Analog Design Engineer, American Microsystems Inc. (AMI), Pocatello, Idaho 83201.
Project Manager and Lead Design Engineer for an ASIC containing a 12 bit ADC, a 12 bit DAC, Two 16 channel analog multiplexers, various gain blocks, and associated digital interface circuitry.

Project Manager and Lead Design Engineer for a switched capacitor filter ASIC containing a 7th order high pass filter with programmable cut off frequencies, and on chip anti-aliasing and smoothing filters. Two 4th order bandpass filters were also included on the ASIC.

Member of a design team for an ASIC containing a variety of CMOS analog cells. Completed the design of the following cells: Track and Hold Amplifier with offset cancellation, Track and Hold Amplifier with charge injection cancellation, and a Comparator with 50ns response time. Also designed charge injection cancellation circuitry for a fully integrated CMOS chopper amplifier. A paper was also written and presented on the chopper amplifier as mentioned below.

*Oct. 1988 to Oct. 1989:* Analog Product Engineer, National Semiconductor, Salt Lake City, Utah
Responsible for switched capacitor filter line. Worked on filter characterization, yield enhancement, wafer sort test program improvement, and test chip development.

*July 1986 to Oct. 1988:* Analog Design and Test Engineer, American Microsystems Inc. (AMI), Pocatello, Idaho 83201.
Design and Test Engineer for an ASIC containing four 13 bit DACs. The design required no trimming or self calibration and has been in production for over five years.

Developed a Group Delay characterization test program using the DSP capabilities of a Teradyne A312 linear test system.Test Engineer for an ASIC containing a 10 bit companding DAC and switched capacitor filters.

PUBLICATIONS: "A Single Analog-to-Digital Converter (ADC) that Converts Two Separate Channels (I and Q) in a Broadband Radio Receiver," Doug Garrity, David Locascio, Chris Cavanagh, M. Nizam Kabir, and Chris Guenther, IEEE Journal of Solid-State Circuits, June 2008.

"Analog-to-Digital Converters for Software Definable Radios," (invited), Matt Miller, Doug Garrity and Pat Rakers, Proceedings of the Software Definable Radio Symposium, October 2004.

Associate Editor for the IEEE Journal of Solid-State Circuits from 2002 to 2005.

Associate Editor for the IEEE Transactions on Circuits and Systems II from 1/1/2002 to 12/31/2002

Guest Editor for the March 1999 and March 2000 Issues of the IEEE Journal of Solid-State Circuits.

Served on the IEEE Custom Integrated Circuits Conference Technical Program Committee from 1994 to 2004. Served for two years as Chairman of the Educational Sessions and for several years as chairman of the Analog Subcommittee.

"High Speed Analog-to-Digital Converters for Embedded Applications," (Invited), Doug Garrity, Proceedings of the 9th NASA Symposium on VLSI Design, November 2000.
"A 10 bit, 40Ms/s Pipelined A/D Converter," Doug Garrity and Syed Aftab, Proceedings of the 1998 International Conference on ASIC, Oct. 1998

“A 10 bit 2Ms/s, 15mW BiCMOS Cyclic A/D Converter,” Doug Garrity and Pat Rakers, Proceedings of the 1996 IEEE BCTM Sept. 1996.

“A 10 bit, 20Ms/s Pipelined A/D Converter,” Doug Garrity and Pat Rakers, Proceedings of the Motorola Technical Enrichment Matrix, Dec. 1994.

“A Low Power, High Frequency, Fully Differential BiCMOS Operational Amplifier,” Doug Garrity, Pat Rakers, and Byron Bynum, Proceedings of the Motorola War on Current Drain Symposium, Sept. 1994.

“A Low Power, 10 bit 2Ms/s Cyclic RSD Analog to Digital Converter,” Pat Rakers, Doug Garrity, and Dave Jaska, Proceedings of the Motorola War on Current Drain Symposium, Sept. 1994

“A Fully Integrated CMOS Chopper Amplifier,” Doug Garrity, Don Ethylene, and Men Khan Young, Proceedings: 1991 IEEE ASIC Conference, P5-2.1, IEEE Catalog #91TH0379-8.

“A Low Power Constant Current Source Based on CMOS Transistors Operating in Weak Inversion,” Doug Garrity and Byron Bynum, Proceedings of Motorola War on Current Drain Symposium, May 1993.

“1.8 Volt Switched Capacitor Filters for Cordless Telephones”, Larry Connell, Neal Henpeck, Doug Garrity, and Jim Caldwell, Proceedings of the Motorola War on Current Drain Symposium, May 1993.

PATENTS: Thirtyone US patents issued, with ~8 additional patents pending. Total patent citations = 477

1. 8,400,339, Correlated-level-shifting and correlated-double-sampling switched-capacitor gains stages, systems implementing the gain stages, and methods of their operation, D. Garrity

2. 8,344,798, Correlated-double-sampling switched-capacitor gain stages, systems implementing the gain stages, and mentods of their operation, D.

Garrity

3. 8,264,393 Current reduction in a single stage cyclic analog to digital converter with variable resolution, D. Garrity, B.Braswell, M.N. Kabir

4. 7,649,957, Non-overlapping multi-stage clock generator system, D. Garrity and M. N. Kabir, 2010, cited by 4

5. 7,589,658, Analog-to-digital converter with variable gain and method thereof, J. Ren, M. Garrard, R. Jones, D. Garrity, 2009, cited by 3.

6. 7,535,391, Analog-to-digital converter having random capacitor assignment and method thereof, B. Newman and D. Garrity, 2009, cited by 4.

7. 7,443,333 Single stage cyclic analog to digital converter with variable resolution, D. Garrity and D. Locascio, 2008, cited by 6.

8. 7,307,572 Programmable dual input switched-capacitor gain stage, D. Garrity, B. Braswell, and D. Locascio, 2007, cited by 23.

9. 7,305,643 Method of tiling analog circuits that include resistors and capacitors, J. McClellan, P. Drennan, D. Garrity, D. Locascio, and M. McGowan, 2007.

10. 7,305,642 Method of tiling analog circuits, J. McClellan, P. Drennan, D. Garrity, D. Locascio, and M. McGowan, 2007, cited by 1

11. 7,289,052 System and method for analog-to-digital conversion, Y. Atriss, B. Braswell, D. Garrity, 2007.

12. 7,282,929 Apparatus for current sensing, Y. Atriss, B. Braswell, and D. Garrity, 2007.10. 7,102,365 Apparatus for current sensing , Y. Atriss, B. Braswell, and D. Garrity, 2007.

13. 7,102,365, "Apparatus for current sensing," Y. Atriss, B. Braswell, and D. Garrity, 2007, cited by 5.

14. 7,064,700 Multi-channel analog to digital converter, D. Garrity, B. Braswell, T. Cassagnes, C. Cavanagh, M. Kabir, and D. Locascio, 2006, cited by 11.

15. 7,015,852 Cyclic analog-to-digital converter, Y. Atriss, B. Braswell, and D. Garrity, 2006, cited by 6

16. 6,967,611 Optimized reference voltage generation using switched capacitor scaling for data converters, A. Atriss, S. Allen, and D. Garrity, 2004, cited by 31.

17. 6,741,194 Methods and apparatus for detecting out-of-range signals in an analog-to-digital converter, T. Cassagnes, D. Garrity, and I. Miller, 2004, cited by 9.

18. 6,535,157 Low power cyclic A/D converter, D. Garrity and P. Rakers, 2003, cited by 32

19. 6,362,770 Dual input switched capacitor gain stage, I. Miller, D. Garrity, T.

Cassagnes, 2002, cited by 20.

20. 6,087,969 Sigma-delta modulator and method for digitizing a signal, T. Stockstad and D. Garrity, 2005, cited by 32+3

21. 5,894,284 Common-mode output sensing circuit, D. Garrity and P. Rakers, 1999, cited by 36.

22. 5,886,562 Method and apparatus for synchronizing a plurality of output clock signals generated from a clock input signal, D. Garrity and D. Bersch, 1999, cited by 12.

23. 5,818,276 Non-overlapping clock generator circuit and method therefor, D. Garrity, P. Rakers, A. Eberhardt, 1998, cited by 13.

24. 5,680,070 Programmable analog array and method for configuring the same, D. Anderson and D. Garrity, 1997, citations 59.

25. 5,644,313 Redundant signed digit A-to-D conversion circuit and method thereof, P. Rakers and D. Garrity, 1997, cited by 25.

26. 5,625,361 Programmable capacitor array and method of programming, D. Garrity, B. Gunter, and D. Bersch, 1997, cited by 12.

27. 5,625,360 Current source for reducing noise glitches generated in a digital to analog converter and method therefor, D. Garrity and P. Rakers, 1997, cited by 50

28. 5,574,457 Switched capacitor gain stage, D. Garrity and P. Rakers, 1996, cited by 44

29. 5,550,503 Circuits and method for reducing voltage error when charging and discharging a capacitor through a transmission gate, D. Garrity, D. Anderson, H. Anderson, B. Gunter and D. Bersch, 1996, cited by 6

30. 5,534,819 Circuit and method for reducing voltage error when charging and discharging a variable capacitor through a switch, B. Gunter, D. Anderson, H. Anderson, D. Bersch and D. Garrity, 1996, cited by 12.

31. 5,525,920 Comparator circuit and method thereof, P. Rakers and D. Garrity, 1996, cited by 10.

AWARDS: Named an IEEE Fellow in 2011. Named a Freescale Fellow (1 of 12 out of 21,000 employees). Named a Freescale Master Innovator. Named a Motorola Dan Noble Fellow (most prestigious recognition possible from Motorola) in 2003. Received the Motorola Distinguished Innovator Award. Named as a member of the Motorola Science Advisory Board Associates in 1999. Received the Semiconductor Research Corporation (SRC) Mahboob Khan Award as Mentor of the Year in 2001. Received the Motorola Liaison Bravo Award for Outstanding Mentoring Contributions to University Research.