Aviral Shrivastava

Professor
School of Computing and Augmented Intelligence
Centerpoint 203-15, 660 Mill Ave, Tempe, Arizona 85281.

Phone/Fax: (480)-727-6509
Email: Aviral.Shrivastava@asu.edu
URL: https://labs.engineering.asu.edu/mps-lab/

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OVERVIEW

Aviral Shrivastava is a full Professor in the School of Computing and Augmented Intelligence (SCAI) at the Arizona State University, where he established and heads the Make Programming Simple Lab. He completed his Ph.D. in Information and Computer Science and from the University of California, Irvine, and bachelor's in Computer Science and Engineering from IIT Delhi.

Research: Prof. Shrivastava's main theme of research in on Making Programming Simple for embedded, accelerated computing, cyber-physical, and quantum computing systems. Prof. Shrivastava and his students work on topics in computer architecture, compilers, machine learning acceleration, quantum computing systems, cyber-physical systems, intelligent transportation, autonomous vehicles.

Publications and Awards: Prof. Shrivastava has co-authored 1 book and has contributed chapters in 4 books. He has more than 200 articles and conference papers in top embedded system journals and conferences, like DAC, ESWEEK, ACM TECS, and ACM TCPS. His papers have received several awards, including a best paper award at VLSI Design conference 2025, nomination for best paper award at DAC 2017, best student paper award at VLSI 2016, second highest ranked paper at LCTES 2010, and best paper candidate ASPDAC 2008. He has published more than 16 papers in DAC (top conference in the field). Overall, his works have received more than 4200 citations, growing at the rate of over 350 citations every year. More than 6 of his papers have been cited more than 100 times. Overall, his h-index[1] is 36 (reference Google Scholar). His inventions have been granted 7 patents, and 4 more applications are pending. Prof. Shrivastava is the recipient of the prestigious 2010 NSF CAREER award. His student's theses were awarded CIDSE outstanding Ph.D. thesis award in 2021 and 2017, and outstanding master's thesis awards in 2010, 2017, and 2022. Prof. Shrivastava's research efforts have been supported by federal agencies (NSF, DOE, NIST), state agencies (SFAZ), and industry.

Teaching and Mentoring: Prof. Shrivastava has mentored 3 postdocs, 10 Ph.D. students, and over 25 Masters students. His students are well placed, including a full Professor at UNIST, South Korea, Assistant Professor at South Dakota School of Mines, Apple (x3), Qualcomm (x2), Nvidia(x2), AMD, Google, Benz, etc. Prof. Shrivastava is currently supervising 1 postdoc, 4 Ph.D., and 7 Masters students. Prof. Shrivastava teaches undergraduate and graduate level courses on computer architecture, cyber-physical, and quantum computing systems. He has consistent student evaluations of over 4/5.

Service: Prof. Shrivastava is currently serving as the Editor-in-Chief of IEEE ESL (Embedded Systems Letters), and in the steering committee of Languages Compilers, Theory and tools for Embedded Systems (LCTES), Embedded Systems Week (ESWEEK), Conference on HW/SW Codesign and System Synthesis (CODES+ISSS). He is serving as the track chair for the Autonomous Systems track at DAC 2025. Previously, he was the General Chair and program chair of (LCTES) 2024 and 2017 respectively. He was the General Chair of Embedded Systems Week (ESWEEK) 2022, which is the top event in the field of Embedded Systems, comprising of 3 conferences, 2 symposia and 7 workshops, 10 education classes, 7 tutorials, special sessions, Ph.D. forum, and student research competitions. His service has been recognized by IEEE through the 2023 IEEE CEDA Outstanding Service Award. He served as program chair of CODES+ISSS 2018, chair of the Design and Applications track of RTSS 2020, and chair of Autonomous Systems track at DAC 2023. He is serving as the associate editor for ACM Transactions of Cyber-Physical Systems (ACM TCPS), ACM Transactions Embedded Computing Systems (ACM TECS). He was associate editor of the IEEE Transactions on Computer Aided Design (IEEE TCAD) 2018-2023. Prof. Shrivastava also serves as the Graduate Program Chair of CS programs at ASU.

BACKGROUND

Academic Preparation

June 2006	**Ph.D.**	**University of California, Irvine, Information and Computer Science** *Thesis: Compiler-in-the-Loop Exploration of Programmable Embedded Systems* Advisors: Profs. Nikil Dutt (chair), Alex Nicolau, and Alex Veidenbaum
May 2002	M.S.	University of California, Irvine, Information and Computer Science
May 1999	B.Tech	Indian Institute of Technology, Delhi, Computer Science and Engineering Thesis: *Hardware Software Partitioning and Synthesis targeted towards FPGA implementation* Advisor: Prof. M. Balakrishnan

Academic Experience

2020 - present	Professor, School of Computing, Informatics and Decision Systems Engineering, Arizona State University.
2012 - 2020	Associate Professor, School of Computing, Informatics and Decision Systems Engineering, Arizona State University.
2012 - 2014	Visiting Faculty, Department of Electrical and Computer Engineering, University of California, Berkeley.
2006 - 2012	Assistant Professor, School of Computing, Informatics and Decision Systems Engineering, Arizona State University.
2002 - 2006	Graduate Research Assistant, Information and Computer Science, University of California, Irvine.
2000 - 2002	Teaching Assistant, Information and Computer Science, University of California, Irvine.

Industrial Experience

July 2014	Faculty Intern at Toyota Motors.
July 2003 – Dec. 2003	Research Intern at Strategic CAD Labs in **Intel** Shrewsbury, MA.
July 2002 – Sept. 2002	Research Intern at **HP Labs** in PICO Group.
Sept. 1999 – June 2000	CAD Engineer at **Philips Semiconductors**, Nijmegen, Netherlands.

Research Interests

i) Accelerated computing for Learning Applications
ii) Architectures, languages, compilers and runtime for fault tolerant computing
iii) Architectures, Languages and Runtime for Time-sensitive applications

Teaching Interests

Computer Organization, Computer Architecture, Embedded Systems, Cyber-Physical Systems, Reliable Computing, Quantum Computing.

AWARDS AND HONORS

- **Editor-in-Chief of IEEE Embedded Systems Letters (ESL)** for 2024-2028.
- **General Chair of Languages Compilers Tools and Theory of Embedded Systems (LCTES)** 2024.
- **General Chair of Embedded Systems Week (ESWEEK)** 2022.
- **15+** papers at Design Automation Conference (DAC) -- the top conference in our field.
- **2023 IEEE CEDA Outstanding Service Award** for serving as the General Chair of Embedded Systems Week 2022. This award is given by the IEEE Council on Electronic Design Automation.
- **2010 NSF CAREER Award** for "Compiler Techniques for Power-Efficient Protection from Soft Errors."
- **2011 Outstanding Junior Researcher**, in the School of Computing Informatics, and Decision Systems Engineering.
- **Best Paper Awards/Candidate**
  - **Best paper award at VLSI Design 2025** "TIPANGLE: Accurate Pan and Tilt angle determination of Traffic Cameras".
  - **Best paper award candidate at DAC 2017** "Crossroads: A Time-Sensitive Autonomous Intersection Management Technique" at DAC 2017 -- the top conference in our field.
  - **Best Poster award** at PhD forum in DAC 2017 for poster titled, "Software Schemes to Tolerate Hardware Faults for Safety-Critical Applications".
  - **Best student paper award at VLSI 2016** "Software Coherence Management on Non-Coherent Cache Multi-cores".
  - **Second highest ranked paper at LCTES 2010**, "Cache Vulnerability Equations for Protecting Data in Processor Caches from Soft Errors".
  - **Best Paper Candidate at ASPDAC 2008**, "SPKM: A Novel Graph Drawing based Algorithm for Application Mapping onto Coarse-Grained Reconfigurable Architecture"
- **My student's awards**
  - **2022 ACM SRC Silver Medal** to Shail Dave for his research on Agile Design of ML Accelerators.
  - **2022 ARCS Scholarship** for my student Edward Andert.
  - **2022 SCAI Outstanding MS thesis** to Sanggu Park for his research on BLAFT – Blame-Free Motion Planning in Hybrid Traffic.
  - **2021 SCAI Outstanding Ph.D. Thesis** in Computer Engineering to Mohammad Khayatian.
  - **2017 SCIDSE Outstanding Ph.D. Thesis** in Computer Engineering to Yooseong Kim.
  - **2012 SCIDSE Outstanding Master's Thesis** in Computer Engineering to Abhishek Risheekesan.
  - **2010 SCIDSE Outstanding Master's Thesis** in Computer Engineering to Seung-chul Jung.
- **102 Rank Nation-wide in JEE 1995**
- **National Talent Search Scholarship,** 1993-1995.

PUBLICATIONS, INTELLECTUAL PROPERTY AND PRESENTATIONS

Summary of Publications and Intellectual Property

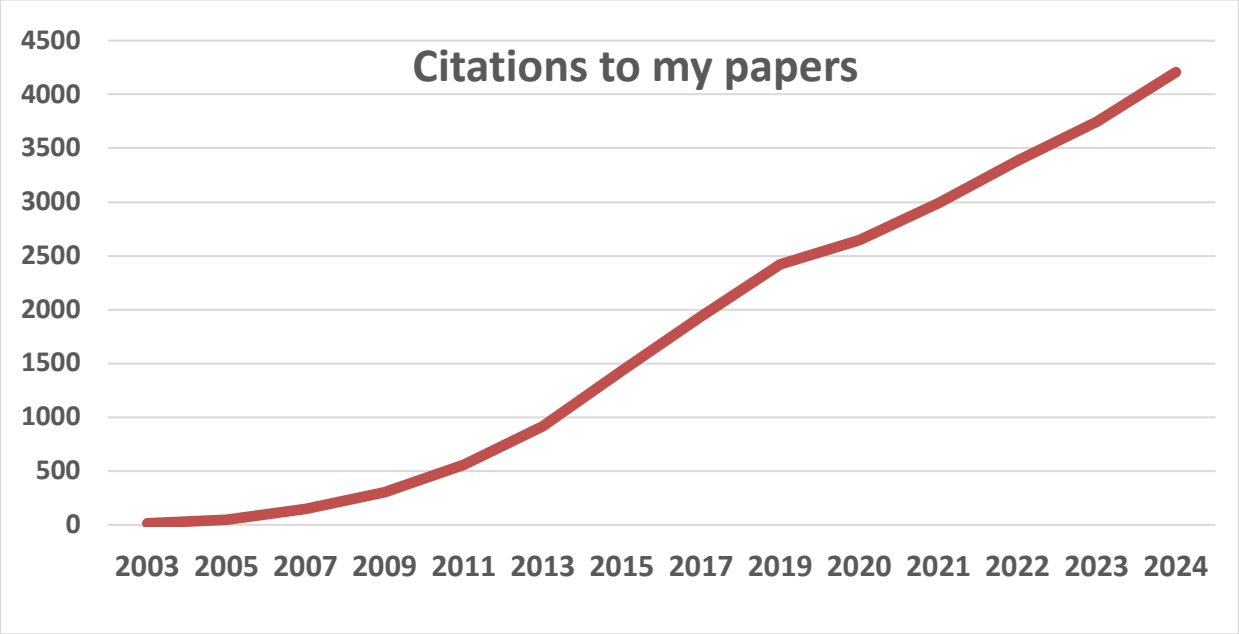

Figure 1: The total number of citations to my work are more than 4200 to date, and increasing at the rate of about 350 new citations every year (source Google scholar)

Highlights:

- 1 Book, 4 book chapters.
- 9 patents granted.
- Over 50 journal articles, 100 conference papers, and 10 workshop papers
- Edited 9 thematic journal issues.
- Over 5 Keynotes, and over 70 invited talks
- 16 papers in DAC – the top conference in design automation.
- More than 40 news articles.
- Best paper award @ VLSI Design 2025
- Best paper candidate @ DAC 2017
- Best poster @ DAC 2017
- Best student paper award @ VLSID 2016
- Second highest rank paper @ LCTES 2010
- Best paper candidate @ ASPDAC 2008

Books Co-Edited

B1. **Book Title: Power-Efficient System Design**
Authors: Preeti Ranjan Panda, **Aviral Shrivastava**, B.V.N. Silpa, and Krishnaiah Gummidipudi
Publisher: Springer
Year: 2010
ISBN: 978-1-4419-6387-1

Book Section Editor

BSE1. **Section Title: Hardware-Software Compilation and Synthesis**
Book Title: Handbook of Hardware Software Codesign
Section Editor: **Aviral Shrivastava**
Section Title: Hardware-Software Compilation and Synthesis
Publisher: Springer
Year: 2017
ISBN: 978-94-017-7266-2

Book Chapters

BC4. **Chapter Title: Techniques to Improve the Resilience of Computing Systems: Architectural layer**
Authors: **Aviral Shrivastava** and Hwisoo So, Jinhyo Kim, Prudhvi Gali, Kyoungwoo Lee
Book title: Cross-Layer Reliability of Computing Systems
Publisher: Springer
Year: 2020
ISBN: 1785617974, 9781785617973

BC3. **Chapter Title: Hardware-Aware Compilation**
Authors: Jian Cai and **Aviral Shrivastava**
Book title: Handbook of Hardware Software Codesign
Publisher: Springer
Year: 2017
ISBN: 978-94-017-7266-2

BC2. **Chapter Title: ADL-Driven Methodologies for Design Automation of Programmable Architectures**
Authors: Prabhat Mishra and **Aviral Shrivastava**
Book title: Processor Description Languages: Applications and Methodologies,
Publisher: Morgan Kaufman
Year: 2007
ISBN: 978-0-12-374287-2

BC1. **Chapter Title: Compiler Aided Design of Embedded Computers**
Authors: **Aviral Shrivastava** and Nikil Dutt
Book title: The Compiler Design Handbook: Optimizations and Machine Code Generation, Second Edition,
Publisher: CRC Press
Year: 2007

ISBN: 978-1-4200-4382-2

Patents Granted

PG9. Patent Title: Systems and methods for fast-mapping of coarse-grained reconfigurable arrays
Inventors: Mahesh Balasubramanian and **Aviral Shrivastava**
US Patent No: US 18603761
Date granted: Sept 2024

PG8. Patent Title: Systems and methods for agile and explainable optimization of efficient hardware/software codesigns for domain-specific computing systems using bottleneck analysis
Inventors: Shail Dave, **Aviral Shrivastava**, Tony Nowatzki.
US Patent No: US 18485811
Date granted: April 2024

PG7. Patent Title: Method for detecting and recovering from soft errors in a computing device
Inventors: Moslem Didehban, **Aviral Shrivastava**, Sai Ram Dheeraj Lokam
US Patent No: US 11449380
Date granted: Sept 2022

PG6. Patent title: Systems and Methods for improved mapping of computational loops on Reconfigurable Architectures
Inventors: Mahesh Balasubramanian and **Aviral Shrivastava**
US Patent No: US 17533663
Date granted: May 2022

PG5. Patent title: Systems and Methods for Intersection Management of Connected Autonomous Vehicles
Inventors: Mohammad Khayatian, **Aviral Shrivastava**, and Mohammadreza Mehrabian
US Patent No: US 11269330
Date granted: March 2022

PG4. Patent Title: Lightweight checkpoint technique for resilience against soft errors
Inventors: Moslem Didehban, Sai Ram Dheeraj Lokam, **Aviral Shrivastava**
US Patent No: US 10997027
Date granted: May 2021

PG3. Patent Title: Systems, methods, and apparatuses for implementing time sensitive autonomous intersection management
Inventors: Edward Andert, Mohammad Khayatian, **Aviral Shrivastava**
US Patent No: US 10437256
Date granted: October 2019

PG2. Patent Title: Heap data management for limited local memory (LLM) multi-core processors
Inventors: Ke Bai and **Aviral Shrivastava**
US Patent No: US9513886B2
Date granted: Dec 2016

PG1. Patent Title: Stack data management for software managed multi-core processors

Inventors: Ke Bai, **Aviral Shrivastava**, and Jing Lu
US Patent No: US9015689B2
Date granted: April 2015

Editor of Thematic Journal Issues

TJ9: **[ACM TECS] Special Issue on Embedded System Security Tutorials**
Co-Editors: **Aviral Shrivastava**, Jian-Jia Chen, and Akash Kumar, Anup Das
Publisher: ACM Transactions on Embedded Computing Systems
June 2023, Article #22, https://doi.org/10.1145/3594872

TJ8: **[IEEE D&T] Report on the 2022 Embedded Systems Week**
Co-Editors: **Aviral Shrivastava** and Sharon X. Hu
Publisher: IEEE Design and Test
Feb 2023, Article #40, https://doi.org/10.1109/MDAT.2022.3222451

TJ7: **[ACM TECS] Special Issue on Embedded System Security**
Co-Editors: **Aviral Shrivastava**, Jian-Jia Chen, Akash Kumar, and Anup Kumar Das
Publisher: ACM Transactions on Embedded Computing Systems
Feb 2023, Article #22, https://doi.org/10.1145/3594872

TJ6: **[IEEE D&T] Report on the 2021 Embedded Systems Week**
Co-Editors: Andreas Gerstlauer and **Aviral Shrivastava**
Publisher: IEEE Design and Test
Feb 2022, Article #39, https://doi.org/10.1109/MDAT.2021.3124759

TJ5: **[Springer RTS] Special Issue on Practical and Robust Design of Real-time Systems**
Co-Editors: Jian-Jia Chen and **Aviral Shrivastava**
Publisher: Springer International Journal on Time-Critical Systems
Sept 2022, Article #58, https://doi.org/10.1007/s11241-022-09390-x

TJ4: **[ACM TCPS] Special Issue on Time in Cyber-Physical Systems**
Co-Editors: **Aviral Shrivastava** and Patricia Derler
Publisher: ACM Transactions on Cyber-Physical Systems
Jan 2021, Article #12, https://doi.org/10.1145/3433948

TJ3: **[ACM TECS] Special Issue on Languages Compilers, Tools and Theory of Embedded Systems 2**
Co-Editors: **Aviral Shrivastava**, Jian-Jia Chen, and Youtao Zhang
Publisher: ACM Transactions on Embedded Computing Systems
Sept 2020, Article #41, https://doi.org/10.1145/3417734

TJ2: **[ACM TECS] Special Issue on Languages Compilers, Tools and Theory of Embedded Systems 1**
Co-Editors: **Aviral Shrivastava**, Jian-Jia Chen, and Youtao Zhang
Publisher: ACM Transactions on Embedded Computing Systems
Sept 2020, Article #30, https://doi.org/10.1145/3417732

TJ1: **[IEEE TMSCS] Special Issue on Accelerated Computing**
Co-Editors: **Aviral Shrivastava** and Fadi Kurdahi

Publisher: IEEE Transactions on Multi-Scale Computing Systems
March 2018, Vol. 4, pages, 1-2, no. 1, doi: 10.1109/TMSCS.2018.2807058

Journal Publications (refereed and archived)

J50. [IEEE Access 2024] IEEE Access
Adversarial Defense on Harmony: Reverse Attack for Robust AI Models Against Adversarial Attacks
Yebon Kim, Jinhyo Jung, Hyunjun Kim, Hwisoo So, Yohan Ko, **Aviral Shrivastava**
Volume 12, November 2024, pages 176485 - 176497

J49. [IEEE IoT] IEEE Internet of Things Magazine
Design Methodology for Robust, Distributed Time-Sensitive Applications
Aviral Shrivastava, Mohammad Khayatian, Bob Iannucci
Volume 7, Issue 1, Jan 2024, pages 104-110.

J48. [IEEE TOC] IEEE Transactions on Computers
CycleBite: Extracting Task Graphs from Unstructured Compute-Programs
Benjamin Willis, **Aviral Shrivastava**, Joshua Mack, Shail Dave, Chaitali Chakrabarti, and John Brunhaver
Volume 73, Issue 1, Jan 2024, pages 221-234.

J47. [ACM TDSC] ACM Transactions on Cyber-Physical Systems
Cooperative Driving of Connected Autonomous vehicle using Responsibility Sensitive Safety Rules: A Control Barrier Functions Approach
Mohammad Khayatian, Mohammadreza Mehrabian, I-Ching Tseng, Chung-Wei Lin, Calin Belta, **Aviral Shrivastava**
Volume 8, Issue 3, July 2024, pages 26.

J46. [MDPI Electronics 2023] MDPI Electronics
gemV-tool: A Comprehensive Soft Error Reliability Estimation Tool for Design Space Exploration
Hwisoo So, Yohan Ko, Jinhyo Jung, Kyoungwoo Lee, **Aviral Shrivastava**
Volume 12, Issue 22, September 2023, pages 4573

J45. [ACM TECS] ACM Transactions on Embedded Computing Systems
B-AWARE: Blockage Aware RSU Scheduling for 5G Enabled Autonomous Vehicles
Matthew Szeto, Edward Andert, **Aviral Shrivastava**, Martin Reisslein, Chung-Wei Lin, Christ Richmond
Volume 2, September 2023, pages 1-23

J44. [IEEE TIV] ACM Transactions on Intelligent Vehicles
Blame-Free Motion Planning in Hybrid Traffic
Sanggu Park; Edward Andert; **Aviral Shrivastava**
April 2023, pages 1-10

J43. [ACM TDSC] ACM Transactions on Dependable and Secure Computing
Generic Soft Error Data and Control Flow Error Detection by Instruction Duplication
Moslem Didehban, Hwisoo So, Prudhvi Gali, **Aviral Shrivastava**, and Kyoungwoo Lee

Vol 21, no. 1, pages 78-92, Feb 2023

J42. [Elsevier M&M] Elsevier Microprocessors and Microsystems
A run-time verification method with consideration of uncertainties for cyber–physical systems
Mohammadreza Mehrabian, Mohammad Khayatian, **Aviral Shrivastava**, Patricia Derler, and Hugo Andrade
Volume 101, September 2023, pages 0141-9331

J41. [ACM TACO] ACM Transactions on Architecture and Code Optimization
EXPERTISE: An Effective Software-level Redundant Multithreading Scheme against hardware faults
Hwisoo So, Moslem Didehban, Yohan Ko, **Aviral Shrivastava**, and Kyoungwoo Lee
Vol 19, issue 4, Sept 2022, pages 1-26

J40. [Elsevier JSA] Elsevier Journal of System Architecture
Root cause analysis of soft-error-induced failures from hardware and software perspectives
Jinhyo Jung, Yohan Ko, Hwisoo So, Kyoungwoo Lee, and **Aviral Shrivastava**
Vol 130, issue 3, Sept 2022, pages 102652

J39. [ACM TCPS] ACM Transactions on Cyber-Physical Systems
Plan B - Design Methodology for Cyber-Physical Systems Robust to Timing Failure
Mohammad Khayatian, Mohamamdreza Mehrabian, Edward Andert, Reese Grimsley, Kyle Liang, Yi Hu, Ian McCormack, Carlee Joe-Wong, Jonathan Aldrich, Bob Iannucci, **Aviral Shrivastava**
Vol 6, issue 3, July 2022, pages 1-39

J38. [PIEEE] Proceedings of the IEEE
Hardware Acceleration of Sparse and Irregular Tensor Computations of ML Models: A Survey and Insights
Shail Dave, Riyadh Baghdadi, Tony Nowatzki, Sasikanth Avancha, **Aviral Shrivastava**, Baoxin Li
vol. 109, issue 10, pages 1706-1752, Oct 2021

J37. [ACM TACO] ACM Transactions on Architecture and Code Optimization (TACO)
SPX64: A Scratchpad Memory for General-Purpose Microprocessors
Abhishek Singh; Shail Dave; PanteA Zardoshti; Robert Brotzman; Chao Zhang; Xiaochen Guo; **Aviral Shrivastava**; Gang Tan; Michael Spear
Vol 18, issue 1, pages 1-26, Mar 2021

J36. [MDPI Electronics] MDPI Electronics
Revisiting Symptom-Based Fault Tolerant Techniques against Soft Errors
Hwisoo So, Moslem Didehban, Yohan Ko, Reiley Jeyapaul, Jongho Kim, Youngbin Kim, Kyoungwoo Lee, **Aviral Shrivastava**
Vol 10, issue 23, Dec 2021.

J35. [ACM TCPS] ACM Transactions on Cyber-Physical Systems
A Survey on Intersection Management of Connected Autonomous Vehicles
Mohammad Khayatian, Mohammadreza Mehrabian, Edward Andert, Rachel Dedinsky, Sarthake Choudhary, Yingyan Lou, and **Aviral Shrivastava**
Vol 4, issue 48, pages 27, August 2020

J34. **[IEEE TCAD] IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**
CRIMSON: Compute-intensive loop acceleration by Randomized Iterative Modulo Scheduling and Optimized Mapping on CGRAs
Mahesh Balasubramanian; **Aviral Shrivastava**
Vol 39, issue 11, pp. 3300-3310, September 2020.

J33. **[ACM TCPS] ACM Transactions on Cyber-Physical Systems**
Crossroads+: A Time-Aware Approach for Intersection Management of Connected Autonomous Vehicles
Mohammad Khayatian, Yingyan Lou, Mohammadreza Mehrabian and **Aviral Shrivastava**
Vol 4, issue 2, pp 20:1--20:28; Nov 2019

J32. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
DMazeRunner: Executing Perfectly Nested Loops on Dataflow Accelerators
Shail Dave, Youngbin Kim, Sasikanth Avancha, Kyoungwoo Lee and **Aviral Shrivastava**
Vol 18, issue 5, pp 70:1--70:27; Oct 2019

J31. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
Control Flow Checking or Not? (for Soft Errors)
Abhishek Rhisheekesan, Reiley Jeyapaul and **Aviral Shrivastava**
Vol 18, issue 1, pp 11:1-11:25; Feb 2019

J30. **[IEEE TR] IEEE Transactions on Reliability**
A Compiler Technique for Processor-Wide Protection from Soft Errors in Multithreaded Environments
Moslem Didehban and **Aviral Shrivastava**
Vol 67, issue. 1, pp 249-263; Mar 2018

J29. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
Timestamp Temporal Logic (TTL) for Time Testing of Cyber-Physical Systems
Mohammadreza Mehrabian, Mohammad Khayatian, **Aviral Shrivastava**, John Eidson, Patricia Derler, Hugo A. Andrade, Ya-Shian Li Baboud, Edward Griffor, Marc Weiss, and Kevin Stanton.
Vol 16, no. 169, pp 169:1--169:20; October 2017

J28. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
Protecting Caches from Soft Errors: A Microarchitect's Perspective
Yohan Ko, Reiley Jeyapaul, Yongbin Kim, Kyoungwoo Lee, and **Aviral Shrivastava**
Vol 16, no. 4, pp; May 2017

J27. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
WCET-Aware Function-Level Dynamic Code Management on Scratchpad Memory
Yooseong Kim, David Broman, and **Aviral Shrivastava**
Vol 16, no. 4, pp; May 2017

J26. **[IEEE TVLSI] IEEE Transactions on VLSI**
Systematic Methodology for the Quantitative Analysis of Pipeline Register Reliability in Embedded Systems
Reiley Jeyapaul, Roberto Flores, Alfonso Avila Ortega, and **Aviral Shrivastava**
Vol 25, no. 2, pp 547-555; June 2016

J25. **[IET CDT] IET Computers and Digital Techniques**
Automatic Management of Software Programmable Memories in Manycore Architectures
Aviral Shrivastava, Nikil Dutt, Jian Cai, Majid Shoushtari, Bryan Donyanavard, Hossein Tajik
Vol 10, no. 6, pp 288-298; November 2016

J24. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
Efficient Code Assignment Techniques for Local Memory on Software Managed Multicores
Jing Lu, Ke Bai, and **Aviral Shrivastava**
Vol 14, issue 4, pages 71:1 – 71:24, December 2015

J23. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
A Software Scheme for Multithreading on CGRAs
Jared Pager, Reiley Jeyapaul and **Aviral Shrivastava**
Vol 14, issue 19, pages 19:1--19:26, January 2015

J22. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
Software-Based Register File Vulnerability Reduction for Embedded Processors
Jongeun Lee and **Aviral Shrivastava**
Vol 13, issue 1, pages 38:1 – 38:20, November 2013

J21. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
A Software-Only Scheme for Managing Heap Data on Limited Local Memory (LLM) Multi-core Processors
Ke Bai and **Aviral Shrivastava**
Vol 13, issue 1, pages 5:1 – 5:18, August 2013

J20. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
Memory Performance Estimation of CUDA Programs.
Yooseong Kim and **Aviral Shrivastava**
Vol 13, issue 21, pages 21:1 – 21:26, September 2013

J19. **[ACM TECS] ACM Transactions on Embedded Computing Systems**
PICA: Processor Idle Cycle Aggregation for Energy Efficient Embedded Systems
Jongeun Lee and **Aviral Shrivastava**
Vol. 11, issue 2, pages 26:1 – 26:27, July 2012

J18. **[IEEE TVLSI] IEEE Transactions on VLSI**
Return Data Interleaving for Multi-channel Embedded CMPs
Fei Hong and **Aviral Shrivastava**, and Jongeun Lee
Vol. 20, issue 7, pages 1351-1354, July 2012

J17. **[IEEE TCAD] IEEE Transactions on Computer Aided Design**
High Throughput Data Mapping for Coarse-Grained Reconfigurable Architectures
Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, and Yunheung Paek
vol. 30, issue 11, pages 1599-1609, November 2011

J16. **[ACM TODAES] ACM Transactions on Design Automation of Embedded Systems**
Memory Access Optimization in compilation for Coarse Grain Reconfigurable Architectures

Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, and Yunheung Paek
Vol. 16, issue 4, pages 42:1--42:27, Octocber 2011

J15. [IEEE TVLSI] IEEE Transactions on VLSI
Static Analysis of Register File Vulnerability
Jongeun Lee and **Aviral Shrivastava**
vol. 30, issue 4, pages 606-616, April 2010

J14. [IEEE TCAD] IEEE Transactions on CAD
A Compiler-Microarchitecture Hybrid Approach to Soft Error Reduction for Register Files
Jongeun Lee and **Aviral Shrivastava**
vol. 29, issue 7, pages 1018-1027, July 2010

J13. [ACM TODAES] ACM Transactions on Design Automation of Embedded Systems
Partitioning Techniques for Partially Protected Caches for Resource-Constrained Embedded Systems
Kyoungwoo Lee, **Aviral Shrivastava**, Ilya Issenin, Nikil Dutt, and Nalini Venkatasubramanian
vol. 15, issue 4, pages 30:1-30:30, October 2010.

J12. [Springer IJPP] International Journal on Parallel Programming
Code Transformations for TLB Power Reduction
Reiley Jeyapaul and **Aviral Shrivastava**
vol. 38, issue 3, pages 254-276, March 2010.

J11. [IEEE TVLSI] IEEE Transactions on VLSI
Reducing Functional Unit Power Consumption and its Variation using Leakage Sensors
Aviral Shrivastava, Deepa Kannan, Sarvesh Bhardwaj, and Sarma Vrudhula
vol. 18, number 6, pages 988-997, June 2010.

J10. [IEEE TCAD] IEEE Transactions on Computer Aided Design
A Software-only solution to use Scratch Pads for Stack Data
Aviral Shrivastava, Arun Kannan, and Jongeun Lee
vol. 28, number 11, pages 1719-1728, Nov 2009.

J9. [IEEE TCAD] IEEE Transactions on Computer Aided Design
Compiler-in-the-Loop Design Space Exploration Framework for Energy Reduction in Horizontally Partitioned Cache Architectures
Aviral Shrivastava, Ilya Issenin, Nikil Dutt, Sanghyun Park, and Yunheung Paek
vol. 28, number 3, pages 461-466, March 2009.

J8. [IEEE TVLSI] IEEE Transactions on VLSI
A Graph Drawing Based Spatial Mapping Algorithm for Coarse-Grained Reconfigurable Architectures
Jonghee W. Yoon, **Aviral Shrivastava**, Sanghyun Park, Minwook Ahn, and Yunheung Paek
vol. 17, number 11, pages 1565-1579, November 2009.

J7. [IEEE TVLSI] IEEE Transactions on VLSI
Partially Protected Caches to Reduce Failures due to Soft Errors in Multimedia Applications
Kyoungwoo Lee, **Aviral Shrivastava**, Ilya Issenin, Nikil Dutt, and Nalini Venkatasubramanian

vol. 17, number 9, pages 1343-1348, September 2009.

J6. **[IFIP DES] IFIP Distributed Embedded Systems**
Data Partitioning Techniques for Partially Protected Caches to Reduce Soft Error Induced Failures
Kyoungwoo Lee, **Aviral Shrivastava**, Nikil Dutt, and Nalini Venkatasubramanian
vol. 271, pages 213-225, 2008.

J5. **[IEEE TCAD] IEEE Transactions on Computer Aided Design**
Register File Power Reduction using Bypass Sensitive Compiler
Sanghyun Park, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek
vol. 27, number 6, pages 1155-1159, June 2008.

J4. **[IEEE TCAD] IEEE Transactions on Computer Aided Design**
Automatic Design Space Exploration of Register Bypasses in Embedded Processors
Aviral Shrivastava, Sanghyun Park, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek
vol. 26, number 12, pages 2102-2115, November. 2007.

J3. **[ACM TODAES] ACM Transactions on Design Automation of Electronic Systems**
Architecture Description Language (ADL)-driven Software Toolkit Generation for Architectural Exploration of Programmable SOCs
Prabhat Mishra, **Aviral Shrivastava**, and Nikil Dutt
vol. 11, number 3, pages 626-658, March 2006.

J2. **[IEEE TVLSI] IEEE Transactions on VLSI**
Retargetable Pipeline Hazard Detection for Partially Bypassed Processors
Aviral Shrivastava, Nikil Dutt, Alex Nicolau, and Eugene Earlie
vol. 14, issue 8, pages 791-801, September 2006.

J1. **[ACM TODAES] ACM Transactions on Design Automation of Electronic Systems**
Compilation Framework for Code Size Reduction using Reduced Bit-width ISAs
Aviral Shrivastava, Partha Biswas, Ashok Halambi, Nikil Dutt and Alex Nicolau
vol. 11, number 1, pages 123-146, January 2006.

Refereed Conference Papers

C104. **[VLSI Design 2025] IEEE International Conference Very Large System Integration and Embedded Systems**
TIPANGLE: Traffic Tracking at City Scale by Pose Estimation of Pan and Tilt Traffic Cameras on Edge Devices,
Shreehari Jagadeesha, Edward Andert, and **Aviral Shrivastava**
Best Paper Award

C103. **[DAC 2024] ACM/IEEE Design Automation Conference**
Maintaining Sanity: Algorithm-based Comprehensive Fault Tolerance for CNNs
Jinhyo Jung, Hwisoo So, Woobin Ko, Sumedh Shridhar Joshi, Yebon Kim, Yohan Ko, **Aviral Shrivastava**, and Kyoungwoo Lee

C102. [DAC 2024] ACM/IEEE Design Automation Conference
Conclave-Secure and Robust Cooperative Perception for Connected Autonomous Vehicle Using Authenticated Consensus and Trust Scoring
Edward Andert, Francis Mendoza, Hans Walter Behrens, and **Aviral Shrivastava**

C101. [ASPLOS 2024] ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
Explainable-DSE: An Agile and Explainable Exploration of Efficient Hardware/Software Codesigns of Deep Learning Accelerators Using Bottleneck Analysis
Shail Dave, Tony Nowatzki, and **Aviral Shrivastava**

C100. [ITSC 2024] IEEE Intelligent Transportation Systems Society Conference
IncidentNet: Traffic Incident Detection, Localization and Severity Estimation with Sparse Sensing
Sai Shashank Peddiraju, Kaustubh Harapanahalli, Edward Andert, and **Aviral Shrivastava**

C99. [DATE 2023] International Conference on Design Automation and Test in Europe (DATE)
Special Session: Learning-Oriented Reliability Improvement of Computing Systems from Transistor to Application Level
Behnaz Ranjbar, Florian Klemme, Paul R. Genssler, Hussam Amrouch, Jinhyo Jung, Shail Dave; Hwisoo So, Kyongwoo Lee, **Aviral Shrivastava**, Ji-Yung Lin, Pieter Weckx, Subrat Mishra, Francky Catthoor, Dwaipayan Biswas, and Akash Kumar

C98. [DATE 2023] International Conference on Design and Test in Europe
Improving Resilience through Learning: From Applications to Transistors
Shail Dave, Hwisoo So, Jinhyo Jung, Kyoungwoo Lee, and **Aviral Shrivastava**

C97. [TechCon 2023] Semiconductor Research Cooperation TECHCON (TECHCON)
Automating the Architectural Execution Modeling and Characterization of Domain-Specific Architectures
Shail Dave, **Aviral Shrivastava**

C96. [MLSys 2023] International Conference on Machine Learning and Systems (MLSys)
GiPH: Generalizable Placement Learning for Adaptive Heterogeneous Computing
Yi Hu, Chaoran Zhang, Edward Andert, Harshul Singh, **Aviral Shrivastava**, James Laudon, Yanqi Zhou, Bob Iannucci, and Carlee Joe-Wong

C95. [ITSC 2022] International Conference on Intelligent Transportation Systems
Accurate Cooperative Sensor Fusion by Parameterized Covariance Generation for Sensing and Localization Pipelines in CAVs
Edward Andert, **Aviral Shrivastava**

C94. [VTS 2022] International Conference on VLSI Test Symposium
Towards an Agile Design Methodology for Efficient, Reliable, and Secure ML Systems
Shail Dave, Alberto Marchisio, Muhammad Abdullah Hanif, Amira Guesmi, **Aviral Shrivastava**, Ihsen Alouani, Muhammad Shafique

C93. [DATE 2022] International Conference on Design Automation and Test in Europe
PathSeeker: A Fast Mapping Algorithm for CGRAs
Mahesh Balasubramanian, **Aviral Shrivastava**

C92. **[DATE 2022] International Conference on Design Automation and Test in Europe**
Compatibility Checking for Autonomous Lane-Changing Assistance Systems
Po-Yu Huang, Kai-Wei Liu, Zong-Lun Li, Sanggu Park, Edward Andert, Chung-Wei Lin, **Aviral Shrivastava**

C91. **[ICCD 2021] IEEE International Conference on Computer Design**
Comprehensive Failure Analysis against Soft Errors from Hardware and Software Perspectives
Yohan Ko, Jin Hyo Jung, Hwisoo So, Kyoungwoo Lee, **Aviral Shrivastava**

C90. **[ICCPS 2021] ACM/IEEE International Conference on Cyber-Physical Systems (ICCPS)**
Cooperative Driving of Connected Autonomous Vehicles Using Responsibility-Sensitive Safety (RSS) Rules
Mohammad Khayatian, Mohammadreza Mehrabian, Harshith Allamsetti, Kai Wei, Po Yu, Chung-Wei Lin, and **Aviral Shrivastava**

C89. **[DATE 2021] Design Automation and Test in Europe**
CHITIN: A Comprehensive In-thread Instruction Replication Technique Against Transient Faults
Hwisoo So, Moslem Didehban, Jinhyo Jung, **Aviral Shrivastava**, and Kyoungwoo Lee

C88. **[IEEE ITSC 2020] IEEE International Conference on Intelligent Transportation System Conference**
R2IM -- Robust and Resilient Intersection Management of Connected Autonomous Vehicles
Mohammad Khayatian, Rachel Dedinsky, Sarthake Choudhary, Mohammadreza Mehrabian, and **Aviral Shrivastava**

C87. **[ICASSP 2020] International Conference on Acoustics, Speech and Signal Processing**
dMazeRunner: Optimizing Convolutions on Dataflow Accelerators
Shail Dave, **Aviral Shrivastava**, Youngbin Kim, Sasikanth Avancha, and Kyoungwoo Lee

C86. **[IPDPS 2020] International Parallel and Distributed Processing Symposium**
Scaling of Union of Intersections for Inference of Granger Causal Networks from Observational Data.
Mahesh Balasubramanian, Trevor Ruiz, Brandon Cook, Mr Prabhat, Sharmodeep Bhattacharyya, **Aviral Shrivastava** and Kristofer Bouchard.

C85. **[DAC 2019] Design Automation Conference**
Software Approaches for In-time Resilience
Moslem Didehban and **Aviral Shrivastava**

C84. **[MEMOCODE 2019] International Conference on Formal Methods and Models for System Design**
Encoding and Monitoring Responsibility Sensitive Safety Rules for Automated Vehicles in Signal Temporal Logic
Mohammad Hekmatnejad, Shakiba Yaghoubi, Adel Dokhanchi, Heni Ben Amor, **Aviral Shrivastava**, Lina Karam and Georgios Fainekos.

C83. **[ICCD 2019] International Conference on Computer Design**
Static Function Prefetching for Efficient Code Management on Scratchpad Memory

Youngbin Kim, Kyoungwoo Lee and **Aviral Shrivastava**

C82. **[DATE 2019] Design Automation and Test in Europe**
A software-level Redundant MultiThreading for Soft/Hard Error Detection and Recovery
Hwisoo So, Moslem Didehban, **Aviral Shrivastava**, and Kyoungwoo Lee

C81. **[VLSI Design 2019] International Conference VLSI Design**
WCET-Aware Stack Frame Management of Embedded Systems using Scratchpad Memories
Yooseong Kim, Mohammad Khayatian and **Aviral Shrivastava**

C80. **[VLSI Design 2019] International Conference VLSI Design**
Efficient Heap Data Management on Software Managed Manycore Architectures
Jinn-Pean Lin, Jing Lu, **Aviral Shrivastava**, and Jian Cai

C79. **[DAC 2018] Design Automation Conference**
RAMP: Resource-Aware Mapping for CGRAs
Shail Dave, Mahesh Balasubramanian, and **Aviral Shrivastava**

C78. **[DAC 2018] Design Automation Conference**
TMA: An Efficient Timestamp-Based Monitoring Approach to Test Timing Constraints of Cyber-Physical Systems.
Mohammadreza Mehrabian, Mohammad Khayatian, Ahmed Mousa, **Aviral Shrivastava**, Ya-Shian Li Baboud, Patricia Derler, Edward Griffor, Hugo A. Andrade, Marc Weiss, John Eidson and Dhananjay Anand.

C77. **[DATE 2018] Design Automation and Test in Europe**
URECA: A Compiler Solution to Manage Unified Register File for CGRAs
Shail Dave, Mahesh Balasubramanian, and **Aviral Shrivastava**

C76. **[DATE 2018] Design Automation and Test in Europe**
LASER: A Hardware/Software Approach to Accelerate Complicated Loops on CGRAs
Mahesh Balasubramanian, Shail Dave, Reiley Jeyapaul and **Aviral Shrivastava**

C75. **[DATE 2018] Design Automation and Test in Europe**
EXPERT: Effective and Flexible Error Protection by Redundant Multithreading
Hwisoo So, Moslem Didehban, Yohan Ko, **Aviral Shrivastava** and Kyoungwoo Lee

C74. **[ICCAD 2017] International Conference on Computer-Aided Design**
NEMESIS: A Software Approach for Computing in Presence of Soft Errors
Moslem Didehban, Dheeraj Lokam, and **Aviral Shrivastava**

C73. **[DAC 2017] Design Automation Conference**
Crossroads – A Time-Sensitive Autonomous Intersection Manager
Edward Andert, Mohammad Khayatian, and **Aviral Shrivastava**
Best Paper Award Candidate

C72. **[DAC 2017] Design Automation Conference**
InCheck: An Integrated Safe and Fast Recovery Scheme from Soft Errors
Moslem Didehban, Dheeraj Lokam, and **Aviral Shrivastava**

C71. **[DAC 2017] Design Automation Conference**
A Testbed to Verify the Timing Behavior of Cyber-Physical Systems
Aviral Shrivastava, Mohammadreza Mehrabian, Mohammad Khayatian, Patricia Derler, Hugo Andrade, Kevin Stanton, Ya-Shian Li-Baboud, Edward Griffor, Marc Weiss and John Eidson

C70. **[DATE 2017] Design Automation and Test in Europe**
Reducing Code Management Overhead in Software Managed Multicores
Jian Cai, Yooseong Kim, Yongbin Kim, **Aviral Shrivastava** and Kyoungwoo Lee

C69. **[CODES+ISSS 2016] International Conference on Hardware/Software Codesign and System Synthesis**
Time in Cyber-Physical Systems
Authors: Aviral Shrivastava, Patricia Derler, Ya-Shian Li-Baboud, Kevin Stanton, Mohammad Khayatian, Hugo Andrade, Marc Weiss, John Eidson and Sundeep Chandhoke

C68. **[ICCAD 2016] International Conference on Computer-Aided Design**
Splitting functions in Code Management on Scratchpad Memories
Yongbin Kim, Jian Cai, Yooseong Kim, Kyoungwoo Lee and **Aviral Shrivastava**

C67. **[MEMSYS 2016] International Symposium on Memory Systems**
Languages Must Expose Memory Heterogeneity
Xiaochen Guo, **Aviral Shrivastava,** Michael Spear and Gang Tan

C66. **[ASAP 2016] International Conference on Application Specific Systems, Architectures and Processors**
Efficient Pointer Management of Stack Data for Software Managed Multicores
Jian Cai and **Aviral Shrivastava**

C65. **[ASAP 2016] International Conference on Application Specific Systems, Architectures and Processors**
gemV: A Validated Toolset for the Early Exploration of System Reliability
Karthik Tanikella, Yohan Ko, Reiley Jeyapaul, Kyoungwoo Lee, and **Aviral Shrivastava**

C64. **[DAC 2016] Design Automation Conference**
nZDC: A Compiler technique for Zero Silent Data Corruption
Moslem Didehban and **Aviral Shrivastava**

C63. **[VLSI Design 2016] International Conference VLSI Design**
Software Coherence Management on Non-Coherent Cache Multi-cores
Jian Cai and **Aviral Shrivastava**
Best Student Paper Award

C62. **[CASES 2015] International Conference on Compilers, Architectures and Synthesis for Embedded Systems**
Optimization of Multi-Channel BCH Error Decoding for Common Cases
Russell Dill and **Aviral Shrivastava**

C61. **[DAC 2015] Design Automation Conference**

Guidelines to Design Parity Protected Write-back L1 Data Cache
Yohan Ko, Reiley Jeyapaul, Yongbin Kim, Kyoungwoo Lee and **Aviral Shrivastava**

C60 [DATE 2015] Design Automation and Test in Europe
Enabling Multi-threaded Applications on Hybrid Shared Memory Manycore Architectures
Tushar Rawat and Aviral Shrivastava

C59. [DATE 2015] Design Automation and Test in Europe
Path Selection Based Acceleration of Conditionals in CGRAs
Shri Hari Rajendran Radhika, Aviral Shrivastava and Mahdi Hamzeh

C58. [RTAS 2015] International Conference on Real-Time Application Systems
A Predictable and Command-Level Priority-Based DRAM Controller for Mixed-Criticality Systems
Hokeun Kim, David Broman, Edward A. Lee, Michael Zimmer, **Aviral Shrivastava** and Junkwang Oh

C57. [DAC 2014] Design Automation Conference
Branch-Aware Loop Mapping on CGRAs
Mahdi Hamzeh, **Aviral Shrivastava**, and Sarma Vrudhula

C56. [RTAS 2014] International Conference on Real-Time Application Systems
WCET-Aware Dynamic Code Management on Scratchpads for Software-Managed Multicores
Yooseong Kim, David Broman, Jian Cai, and **Aviral Shrivastava**

C55. [CODES+ISSS 2013] International Conference on Hardware/Software Codesign and System Synthesis
CMSM: An Efficient and Effective Code Management for Software Managed Multicores
Ke Bai, Jing Lu, **Aviral Shrivastava**, and Bryce Holton

C54. [DAC 2013] Design Automation Conference
SSDM: Smart Stack Data Management for Software Managed Multicores (SMMs)
Jing Lu, Ke Bai and **Aviral Shrivastava**

C53. [DAC 2013] Design Automation Conference
RegiMap: Register-Aware application mapping on coarse-grained reconfigurable architectures (CGRAs)
Mahdi Hamzeh, **Aviral Shrivastava**, and Sarma Vrudhula

C52. [DATE 2013] Design Automation and Test in Europe
Automatic and Efficient Heap data management for Limited Local Memory Multicore Architectures
Ke Bai and **Aviral Shrivastava**

C51. [GLSVLSI 2012] Great Lakes Symposium on VLSI
Fast and Energy-Efficient Constant-Coefficient FIR Filters Using Residue Number System
Piotr Patronik, Krzysztof Berezowski, Stanislaw Piestrak, Janusz Biernat and **Aviral Shrivastava**

C50. [DAC 2012] Design Automation Conference
EPIMap: Using Epimorphism to Map Applications on CGRAs

Mahdi Hamzeh, **Aviral Shrivastava**, and Sarma Vrudhula

C49. [GLSVLSI 2012] Great Lakes Symposium on VLSI
An Efficient RNS Reverse Converter for a New Five-Moduli Special Set
Piotr Patronik, Krzysztof Berezowski, Stanislaw Piestrak, Janusz Biernat and **Aviral Shrivastava**

C48. [CODES+ISSS 2011] International Conference on Hardware/Software Codesign and System Synthesis
Branch Penalty Reduction on IBM Cell SPUs via Software Branch Hinting
Jing Lu, Yooseong Kim, and **Aviral Shrivastava**

C47. [ICPP 2011] International Conference on Parallel Processing
UnSync: A Soft Error Resilient Redundant Multicore Architecture
Reiley Jeyapaul, **Aviral Shrivastava**, Fei Hong, Abhishek Rhisheekesan, and Kyoungwoo Lee

C46. [ICPP 2011] International Conference on Parallel Processing
Enabling Multi-threading on CGRAs
Aviral Shrivastava, Jared Pager, Reiley Jeyapaul, Mahdi Hamzeh, and Sarma Vrudhula

C45. [CASES 2011] International Conference on Compilers, Architectures and Synthesis for Embedded Systems
Smart Cache Cleaning: Energy-Efficient Vulnerability Reduction in Embedded Processors
Reiley Jeyapaul and **Aviral Shrivastava**

C44. [CASES 2011] International Conference on Compilers, Architectures and Synthesis for Embedded Systems
Vector Class on Limited Local Memory (LLM) Multi-core Processors
Ke Bai, Di Lu, and **Aviral Shrivastava**

C43. [ASAP 2011] International Conference on Application Specific Systems, Architectures and Processors
Stack Data Management for Limited Local Memory (LLM) Multi-core Processors
Ke Bai, **Aviral Shrivastava,** and Saleel Kudchadker

C42. [DAC 2011] Design Automation Conference
CuMAPz: A Tool to Analyze Memory Access Patterns in CUDA
Yooseong Kim and **Aviral Shrivastava**

C41. [ISLPED 2011] International Symposium on Low Power Electronics and Design
Fast and Energy-Efficient Constant-Coefficient FIR Filters Using Residue Number System
Piotr Patronik, Krzysztof Berezowski, Stanislaw Piestrak, Janusz Biernat and **Aviral Shrivastava**

C40. [VLSI 2011] International Conference on VLSI Design
LA-LRU: A Latency-Aware Replacement Policy for Variation Tolerant Caches
Aarul Jain, **Aviral Shrivastava**, and Chaitali Chakrabarti

C39. [CODES+ISSS 2010] International Conference on Hardware/Software Codesign and System Synthesis
Heap Data Management for Limited Local Memory (LLM) Multi-core Processors

Ke Bai and **Aviral Shrivastava**

C38. **[ASAP 2010] International Conference on Application-specific Systems, Architectures and Processors**
Dynamic Code Mapping for Limited Local Memory Systems
Seung chul Jung, **Aviral Shrivastava**, and Ke Bai

C37. **[SCOPES 2010] International Conference on Software and Compilers for Embedded Systems**
B2P2: Bounds Based Procedure Placement for Instruction TLB Power Reduction in Embedded Systems
Reiley Jeyapaul and **Aviral Shrivastava**

C36. **[LCTES 2010] International Conference on Languages, Compilers and Tool support for Embedded Systems**
Cache Vulnerability Equations for Protecting Data in Processor Caches from Soft Errors
Aviral Shrivastava, Jongeun Lee, and Reiley Jeyapaul
Second Highest Ranked Paper

C35. **[LCTES 2010] International Conference on Languages, Compilers and Tool support for Embedded Systems**
Operation and Data Mapping for CGRAs with Multi-bank Memory
Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, Jonghee Yoon, and Yunheung Paek

C34. **[DATE 2010] International Conference on Design Automation and Test in Europe**
Power-Accuracy Tradeoffs in Human Activity Detection
Jeffrey Boyd, Hari Sundaram, and **Aviral Shrivastava**

C33. **[HIPEAC 2009] International Conference on High-Performance Embedded Architectures and Compilers**
Memory-Aware Application Mapping on Coarse Grain Reconfigurable Arrays
Yongjoo Kim, Jongeun Lee, **Aviral Shrivastava**, Jonghee Yoon, and Yunheung Paek

C32. **[CASES 2009] International Conference on Compilers, Architectures and Synthesis for Embedded Systems**
Exploiting Residue Number System for Power-Efficient Digital Signal Processing in Embedded Processors
Rooju Chokshi, Krzysztof Berezowski, and **Aviral Shrivastava**

C31. **[LCTES 2009] Languages, Compilers and Tool support for Embedded Systems**
A Compiler Optimization to Reduce Soft Errors in Register Files
Jongeun Lee and **Aviral Shrivastava**

C30. **[VLSI-SOC 2009] International Conference on Very Large Scale Integration**
Adaptive Reduced Bit-width Instruction Set Architecture (adapt-RISA)
Sandro Neves Soares, Ashok Halambi, **Aviral Shrivastava**, Flavio Rech Wagner, and Nikil Dutt

C29. **[DATE 2009] International Conference on Design Automation and Test in Europe**
Static Analysis to Mitigate Soft Errors in Register Files
Jongeun Lee and **Aviral Shrivastava**

C28. **[DATE 2009] International Conference on Design Automation and Test in Europe**
FSAF: File System Aware Flash Translation Layer for NAND Flash Memories
Sai Mylavarapu, **Aviral Shrivastava**, and Jongeun Lee

C27. **[ASPDAC 2009] Asia and South Pacific Design Automation Conference**
A Software Solution for Dynamic Stack Management on Scratch Pad Memory
Arun Kannan, **Aviral Shrivastava**, Amit Pabalkar and Jongeun Lee

C26. **[ASPDAC 2009] Asia and South Pacific Design Automation Conference**
Compiler-Managed Register File Protection for Energy-Efficient Soft Error Reduction
Jongeun Lee and **Aviral Shrivastava**

C25. **[VLSI 2009] International Conference on VLSI Design**
Code Transformations for TLB Power Reduction
Reiley Jeyapaul and **Aviral Shrivastava**

C24. **[CODES+ISSS 2008] International Conference on Hardware/Software Codesign and System Synthesis**
Static Analysis of Processor Stall Cycle Aggregation
Jongeun Lee and **Aviral Shrivastava**

C23. **[HIPC 2008] International Conference on High Performance Computing**
SDRM: Simultaneous Determination of Regions and Function-to-Region Mapping for Scratchpad Memories
Amit Pabalkar, **Aviral Shrivastava**, Arun Kannan, and Jongeun Lee

C22. **[ACM MM 2008] ACM International Conference on Multimedia**
Mitigating the Impact of Hardware Failures on Multimedia Applications - A Cross-Layer Approach
Kyoungwoo Lee, **Aviral Shrivastava**, Minyoung Kim, Nikil Dutt and Nalini Venkatasubramanian

C21. **[DIPES 2008] IFIP Conference on Distributed and Parallel Embedded Systems**
Partitioning Techniques for Partially Protected Caches to Reduce Soft Error Induced Failures
Sanghyun Park, Kyoungwoo Lee, **Aviral Shrivastava**, Nikil Dutt and Nalini Venkatasubramanian

C20. **[DATE 2008] International Conference on Design Automation and Test in Europe**
Hiding Cache Miss Penalty Using Priority-based Execution for Embedded Processors
Sanghyun Park, **Aviral Shrivastava**, and Yunheung Paek

C19. **[ASPDAC 2008] Asia and South Pacific Design Automation Conference**
SPKM: A Novel Graph Drawing based Algorithm for Application Mapping onto Coarse-Grained Reconfigurable Architecture
Jonghee W. Yoon, **Aviral Shrivastava**, Sanghyun Park, Minwook Ahn, and Yunheung Paek
Best Paper Candidate

C18. **[ASPDAC 2008] Asia and South Pacific Design Automation Conference**
A Compiler-in-the-Loop Framework for Exploration of Horizontally Partitioned Caches
Aviral Shrivastava, Ilya Issenin, and Nikil Dutt

C17. **[VLSI 2008] International Conference on VLSI Design**
PTSMT: A Tool for Cross-Level Power, Performance and Thermal Exploration
Deepa Kannan, Aseem Gupta, **Aviral Shrivastava**, Fadi Kurdahi, and Nikil Dutt

C16. **[VLSI 2008] International Conference on VLSI Design**
Temperature and Process Variations aware Power Gating of Functional Units
Deepa Kannan, Vipin Mohan, Sarvesh Bhardwaj, **Aviral Shrivastava** and Sarma Vrudhula

C15. **[VLSI 2008] International Conference on VLSI Design**
Power Reduction of Functional Units considering Temperature and Process Variations
Deepa Kannan, Sarvesh Bhardwaj, **Aviral Shrivastava** and Sarma Vrudhula

C14. **[CODES+ISSS 2007] International Conference on Hardware - Software Codesign and System Synthesis**
Smart Driver for Power Reduction in Next Generation Bi-Stable Electrophoretic Display Technology
Michael A. Baker, **Aviral Shrivastava** and Karamvir Chatha

C13. **[DATE 2007] International Conference on Design Automation and Test in Europe**
Functional and Timing Validation of Partially Bypassed Processors
Qiang Zhu, **Aviral Shrivastava** and Nikil Dutt

C12. **[ICC 2007] International Conference on Communications**
Robust Localization in Wireless Sensor Networks through the Revocation of Malicious Anchors
Satyajayant Mishra, Guoliang Xue and **Aviral Shrivastava**

C11. **[CASES 2006] International Conference on Compiler Architecture and Synthesis for Embedded Systems**
Mitigating Soft Error Failures for Multimedia Applications by Selective Data Protection
Kyoungwoo Lee, **Aviral Shrivastava**, Ilya Issenin, Nikil Dutt, and Nalini Venkatasubramanian

C10. **[LCTES 2006] Language, Compilers and Tool for Embedded Systems**
Bypass Aware Instruction Scheduling for Register File Power Reduction
Sanghyun Park, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek.
Best Paper Candidate

C9. **[DATE 2006] International Conference on Design Automation and Test in Europe**
Automatic Generation of Operation Tables for Fast Exploration of Bypasses in Embedded Processors
Sanghyun Park, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau, Eugene Earlie, and Yunheung Paek.

C8. **[CASES 2005] International Conference on Compiler Architecture and Synthesis for Embedded Systems**
Compilation Techniques for Energy Reduction in Horizontally Partitioned Cache Architectures
Aviral Shrivastava, Ilya Issenin, and Nikil Dutt.

C7. **[CODES+ISSS 2005] International Conference on Hardware - Software Codesign and System Synthesis**
Aggregating Processor Free Time for Energy Reduction
Aviral Shrivastava, Eugene Earlie, Nikil Dutt and Alex Nicolau.

C6. **[DATE 2005] International Conference on Design Automation and Test in Europe**
PBExplore: A Framework for Compiler-in-the-Loop Exploration of Partial Bypassing in Embedded Processors
Aviral Shrivastava, Nikil Dutt, Alex Nicolau and Eugene Earlie

C5. **[CODES+ISSS 2004] International Conference on Hardware - Software Codesign and System Synthesis**
Operation Tables for Scheduling in the Presence of Incomplete Bypassing
Aviral Shrivastava, Eugene Earlie, Nikil Dutt, Alex Nicolau.

C4. **[ASPDAC 2004] Asia South-Pacific Design Automation Conference**
Energy Efficient Code Generation using rISA
Aviral Shrivastava, Nikil Dutt.

C3. **[ISSS 2002] International Symposium on System Synthesis**
A Design Space Exploration Framework for Reduced Bit-width Instruction Set Architecture (rISA) Design
Ashok Halambi, **Aviral Shrivastava**, Partha Biswas, Nikil Dutt, Alex Nicolau.

C2. **[DATE 2002] International Conference on Design Automation and Test in Europe**
An Efficient Compiler Technique for Code Size Reduction using Reduced Bit-width ISAs
Ashok Halambi, **Aviral Shrivastava**, Partha Biswas, Nikil Dutt, Alex Nicolau.

C1. **[VLSI 2000] International Conference on VLSI Design**
Optimal Hardware-Software Partitioning of Concurrent Sequence Flow Graphs
Aviral Shrivastava, Mohit Kumar, Sanjiv Kapoor, Shashi Kumar, M. Balakrishnan

Other Publications (arXiv preprints, Workshops, Tutorials, Education classes etc.)

O11. **[arXiv] arXiv Preprint**
Quantum Polar Metric Learning: Efficient Classically Learned Quantum Embeddings
Vinayak Sharma and **Aviral Shrivastava**
December 2023, arXiv:2312.01655

O10. **[arXiv] arXiv Preprint**
DSP-MLIR: A Dialect for Digital Signal Processing
Abhinav Kumar, Atharva Khedkar and **Aviral Shrivastava**
August 2024, arXiv:2408.11205

O9. **[CASES 2024] International Conference on Compilers Architecture and Synthesis for Embedded Systems**
Education Class: Primer on Data in Quantum Machine Learning
Vinayak Sharma and **Aviral Shrivastava**
September 2024, pages 19-20

O8. **[SNN 2022] Workshop on Sparsity in Neural Networks**
Efficient Sparse NN Processing on Hardware Accelerators: Survey and Insights
Shail Dave, **Aviral Shrivastava**

O7. **[IPDPS Ph.D. Forum 2022] Ph.D. Forum at International Parallel & Distributed Processing Symposium**
Accelerator Design 2.0: Agile, Efficient, Explainable, and Sustainable
Shail Dave, **Aviral Shrivastava**

O6. **[ROAD4NN 2022] Workshop on Research Open Automatic Design for Neural Networks**
Agile and Explainable Exploration of Efficient Hardware/Software Codesigns of Deep Learning Accelerators
Shail Dave, **Aviral Shrivastava**

O5. **[ACM SIGDA University Demonstration] University Demonstration at Design Automation Conference**
Efficient Hardware/Software Codesigns of NPUs in Minutes!
Shail Dave, **Aviral Shrivastava**

O4. **[ECOOP 2021] Workshop on Implementation, Compilation, Optimization of OO Languages, Programs and Systems**
A Framework and DSL for Distributed, Energy-constrained, and Time-sensitive Applications
Kyle Liang, Reese Grimsley, Eve Hu, Edward Andert, Mohammad Khayatian, **Aviral Shrivastava,** Carlee Joe-Wong, Jonathan Aldrich, and Bob Iannucci

O3. **[ASD 2018] Workshop on Autonomous Systems Design**
A Dependable Detection Mechanism for Intersection Management of Connected Autonomous Vehicles
Rachel Dedinsky, Mohmmad Khayatian, Mohammadreza Mehrabian and **Aviral Shrivastava**

O2. **[WASP 2007] Workshop on Application-Specific Processors**
Power Conscious Mapping onto Coarse-Grained Reconfigurable Architectures using Graph Drawing based Algorithm
Jonghee W. Yoon, **Aviral Shrivastava**, Sanghyun Park, Minwook Ahn and Yunheung Paek

O1. **[SCOPES 2001] International Workshop on Software and Compilers for Embedded Systems**
A Customizable Compiler Framework for Embedded Systems
Ashok Halambi, **Aviral Shrivastava**, Nikil Dutt, Alex Nicolau.

Summary of Presentations

Invited Keynotes - 6
Invited Presentations - 78

Invited Keynotes

K6. **[Workshop on Quantum Computing (QuCAM 2024)]**
Title: Quantum Computing: Circuits, Algorithms, and Machine Learning
NIT Rourkela, December 2024
Attendees: 100

K5. **[International Conference on Intelligent Transportation and Smart Cities (ITSC-2022)]**
Title: Towards Connected and Safe Autonomous Vehicle
Online, February 2023
Attendees: 200

K4. **[Faculty Development Program, YCCE]**
Title: Towards Connected and Safe Autonomous Vehicle
Yashwantrao Chauhan College of Engineering, April 2022
Attendees: 200

K3. **[International Symposium on VLSI Design and Test (VDAT-2021)]**
Title: Towards Connected and Safe Autonomous Vehicle
NIT Surat, India, November 2020
Attendees: 200

K2. **[SGBIT International E-Conference on Applications of Intelligent Computing (ICAIC-2020)]**
Title: Traffic Intersection of Autonomous Vehicles
Belgavi, India. November 2020
Attendees: 200

K1. **[International Conference on Nanoelectronic and Information Systems (INIS)]**
Title: Time for Cyber-Physical Systems
Bhopal, India. December 2017
Attendees: 200

Invited Presentations

T78. **[VLSID] Very Large-Scale Integration Design and Embedded Systems International Conference 2025**
Tutorial: Primer on Data in Quantum Machine Learning

T77. **[CASES] International Conference on Compilers Architecture and Synthesis of Embedded Systems 2024**
Education Class: Primer on Data in Quantum Machine Learning

T76. **[University of Erlangen] Nuremberg, Germany Sept 2023**
Agile and Explainable AI Hardware/Software Codesign Exploration

T75. **[IBM] Almadena, CA. June 2023**
Agile and Explainable AI Hardware/Software Codesign Exploration

T74. **[Intel] Santa Clara, CA. May 2023**
Agile and Explainable AI Hardware/Software Codesign Exploration

T73. **[Mathworks] Boston, MA. May 2021**
Time-sensitive Cyber-Physical Systems

T72. **[Science Olympiad] ASU May 2021**
Autonomous Vehicle Research

T71. **[Intel] Santa Clara, CA. Nov 2020**
Sparse DNN Acceleration

T70. **[Intel] Santa Clara, CA. Oct 2020**
Hardware Software Model Codesigns for Efficient Dense/Sparse DNN Acceleration

T69. **[UCI Computer Science Seminar] Irvine, CA. Feb 2020**
Make Programming Simple Again

T68. **[Intel] Hilsboro, OR. Nov 2019**
Timing in Autonomous Vehicles

T67. **[ARM Research Summit] Austin, TX. Sept 2019**
Efficient Execution of Machine Learning Kernels on Dataflow Accelerators

T66. **[Intel] Santa Clara, CA. Sept 2019**
Efficient Execution of Machine Learning Kernels on Dataflow Accelerators

T65. **[TOMNET Transportation Seminar] ASU. Feb 2019**
Time for Cyber-Physical Systems

T64. **[Karlsruhe Institute of Technology] Karlsruhe, Germany. June 2019**
Software Schemes for Resilience Against Soft Errors

T63. **[NIST Workshop on Consensus Safety Measurement Methodologies for ADS-Equipped Vehicles] Gaithersburg, MA. June 2019**
Programmable Test-Track for AVs

T62. **[UCLA] Los Angeles, CA. May 2019**
Resurgence of Dataflow Accelerators

T61. **[Intel Meeting] Bangalore, India. Feb 2019**
Executing DNNs on Dataflow Accelerators

T60. **[Future Chips Workshop] Beijing, China. December 2018**
Acceleration Beyond GPUs

T59. **[Intel Summit] Santa Clara, CA. October 2018**
Acceleration Beyond GPUs

T58. **[ARM Summit] Cambridge, UK. September 2018**
Acceleration Beyond GPUs

T57. **[Intel] Boston MA. February 2018**
Software Schemes for Soft Errors

T56. **[International Workshop on Cross-Layer Resilience (IWCR)] Seoul, South Korea. May 2017**
Software Schemes for Soft Errors

T55. **[Patton Boggs] San Francisco, CA. May 2017**
Autonomous Vehicles: Is our Infrastructure Ready?

T54. **[Workshop on Synchronization and Timing Systems] San Jose, CA. April 2017**
Time-testing of Cyber-Physical Systems

T53. **[University of Michigan, Ann Arbor] Ann Arbor, MI. February 2017**
Software Solutions for Soft Errors

T52. **[Mathworks] Boston, MA. June 2016**
Time in Cyber-Physical Systems

T51. **[ARM Inc] San Jose, CA. June 2016**
Software Techniques for Protection Against Soft Errors

T50. **[ARM Inc] Austin, TX. May 2016**
Acceleration beyond GPUs

T49. **[NIST] Gaithersburg, MD. May 2016**
Time Testing in Cyber-Physical Systems

T48. **[Council on Social Work Education] Denver, CO. Oct 2015**
Cell-phone based Interventions for Violence Prevention

T47. **[Qualcomm Inc.] San Jose, CA. March 2015**
Compilers for Scratchpad based Manycore Processors

T46. **[University of California, Berkeley] Berkeley, CA. Feb 2014**
Correct-by-Construction for Cyber-Physical Systems at CHESS Symposium

T45. **[New York University] New York, NY. Oct 2014**
Control Flow Checking or Not (for Soft Errors)

T44. **[Intel] Portland, OR. Aug 2014**
Compilers for Scratchpad based Manycore Processors

T43. **[University of Pittsburg] Pittsburg, PA. March 2014**
Beyond the Hill of Multicores, likes the valley of Accelerators

T42. **[University of California, Berkeley] Berkeley, CA. Feb 2014**
Correct-by-Construction for Cyber-Physical Systems at CHESS Symposium

T41. **[University of Michigan, Ann Arbor] Ann Arbor, MI, Oct. 2013**
Compilation for Scratchpad based Manycore Architectures.

T40. **[Reservoir Labs, New York] New York, NY, Oct. 2013**

Beyond the Hill of Multicores, likes the valley of Accelerators

T39. **[AMD, San Jose] San Jose, CA, June 2013**
Compiling for Scratchpad Memory

T38. **[University of California, Berkeley] Berkeley, CA, Oct. 2012**
Beyond the Hill of Multicores, lies the valley of Accelerators

T37. **[University of Maryland, College Park] College Park, MA, Sept. 2012**
Beyond the Hill of Multicores, lies the valley of Accelerators

T36. **[L.G. Electronics] Seoul, South Korea, Aug. 2012**
Beyond the Hill of Multicores, lies the valley of Accelerators

T35. **[Samsung Electronics] Suwon, South Korea, Aug. 2012**
Beyond the Hill of Multicores, lies the valley of Accelerators

T34. **[Seoul National University] Seoul, South Korea, Aug. 2012**
Beyond the Hill of Multicores, lies the valley of Accelerators

T33. **[University of California, Los Angeles] Los Angeles, CA, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T32. **[Purdue University] West Lafayette, IN, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T31. **[University of Pennsylvania] Philadelphia, PA, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T30. **[University of California, San Diego] San Diego, CA, April 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T29. **[Georgia Institute of Technology] Atlanta, GA, March 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T28. **[University of Texas at Austin] Austin, TX, March 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T27. **[Columbia University] New York, NY, March 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T26. **[IIT Ropar] Ropar, India, 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T25. **[IIT Delhi] New Delhi, India, 2011**
Multi-core Computing Challenge: Missing Memory Virtualization

T24. **[Texas Instruments] Houston, TX, 2010**
Compilation for Hybrid Cache and SPM Memory Hierarchy

T23. **[Marvell Semiconductors] Chandler, AZ, 2010**
Research on Low-Power Compilation

T22. **[THQ Studios] Phoenix, AZ, 2010**
Compilation for IBM Cell

T21. **[Professional Course] Tempe, AZ 2009**
Multi-core Programming - A 2-day Professional Course

T20. **[Caltech Center for Advanced Computing Research] Pasadena, California, 2009**
Compiler-Aided Soft Error Protection of Register File

T19. **[Space Mission Challenges SMC-IT] Pasadena, CA, 2009**
Compiler-enabled Power-Efficient Register File Protection

T18. **[Texas Instruments] Houston, TX 2009**
Multi-core Computing Challenge: Missing Memory Virtualization

T17. **[IBM Research Labs] New Delhi, India 2009**
Multi-core Computing Challenge: Missing Memory Virtualization

T16. **[Sagar Institute of Technology] Bhopal, India 2008**
The Growth of Computing and the Multi-core challenges

T15. **[Compiler Assisted SoC Assembly Workshop] Atlanta, GA, 2008**
Scratch Pad Memories: Life beyond Embedded Systems

T14. **[BK21 Workshop] Seoul, South Korea, 2008**
Compiler and Microarchitectural Techniques for Leakage Reduction

T13. **[ETRI] Seoul South Korea, 2008**
Application Mapping onto Coarse-Grain Reconfigurable Architectures

T12. **[Microsoft Research] Redmond, WA, 2007**
Compiler and Microarchitectural Techniques for Low Leakage

T11. **[LSI Systems] San Jose, 2007**
Compiler and Microarchitectural Techniques for Low Leakage

T10. **[NSF IUCRC Workshop] ASU, Tempe, AZ, 2007**
Compiler Techniques for Power Reduction in Embedded Processors

T9. **[Coware Inc.] Noida, India, 2007**
Architecture-Sensitive Compiler Techniques for Energy Reduction

T8. **[IIT Delhi] New Delhi, India, 2007**
Compiler-in-the-Loop Exploration of Embedded Systems

T7. **[Indian Institute of Sciences] Bangalore, India, 2007**
Compiler-in-the-Loop Exploration of Embedded Systems

T6. **[Workshop on Compiler Assisted SoC Assembly] Seoul National University, South Korea, 2006**
Compiler-assisted Processor Exploration and Design

T5. **[Apple Inc.] Cupertino, CA, 2006**
Architecture Sensitive Compilation Techniques for Energy Reduction

T4. **[Seoul National University] South Korea, 2006**
Architecture Sensitive Compilation Techniques for Energy Reduction

T3. **[Optimizing Compiler Assisted SoC Assembly Workshop] Seoul, South Korea, 2005**
Compiler-in-the-Loop Exploration of Programmable SoCs

T2. **[VSSAD, Intel] Hudson, MA, 2005**
Compiler-in-the-loop Design Space Exploration of XScale Microarchitectures using EXPRESSION

T1. **[Strategic CAD Labs, Intel] Shrewsbury, MA, 2003**
Compiler Optimizations for Performance and Energy Improvements in Simple In-order Processors

In the Press

P42. [January 2024] [ABC15 Arizona News]
What to know about Waymo's plan to drive on freeways

P41. [August 2023] [ASU news, ASU alumni news, ASU Ira Fulton Engineering news, ASU School of Computing and AI News, ACM (Association of Computing Machinery) Tech News, Communications of the ACM (CACM) news]
Opening the black box

P39. [March 2023] StatePress]
Mile by Mile

P38. [July 2023] [ASU Full Circle]
ASU research ensures autonomous vehicle safety, reliability.

P37. [November 2022] [IEEE Bridge]
Design Space Modeling and Optimizations for Dataflow Accelerators

P36. [October 2022] [ASU News]
The STAM Center and School of Computing and Augmented Intelligence host ESWEEK event

P35. [October 2022] [ASU News]
Digital license plate messages let drivers express themselves

P34. [March 2022] [ASU News]

Innovative helper and assistive robots mark ASU's celebration of National Robotics Week

P33. [June 2021] [ASU Engineering News]
First IoT Expert Curiosity University T-Mobile Cohort

P32. [May 2021] [ASU News]
Essential reading: Books to expand your perspective

P31. [July 2021] [CACM] [ASU News] **[Full Circle]**
Connected Autonomous Vehicles make Intersections Safer
Connected Autonomous Vehicles make Intersections Safer
Connected Autonomous Vehicles make Intersections Safer

P30. [Aug 2020] **[Full Circle]**
Smart Transportation Systems Need To Reckon With Rogues
Smart transportation systems need to reckon with rogues

P29. [Dec 2019] **[Full Circle]**
A Soft Approach to a Hard Problem in Autonomous Vehicles

P28. [June 2019] **[National Institute for Standards and Technology (NIST)]**
Programmable Test track for AVs

P27. [February 2019] **[Fox News]**
Digital license plates that cost whopping $499 now an option for Arizona drivers.

P26. [January 2019] **[ASU Inner Circle]** **[ASU InTheLoop]**
Aviral presented at ASU Transportation Seminar on "Time in cyber-physical systems".
Transportation Seminar: Time in cyber-physical systems, January 31
Transportation Seminar: Time In Cyber-Physical Systems, January 31

P25: [September 2018] [**InsideHPC**] [**ARM Summit 2018**]
Energy efficient acceleration of residual neural networks using CGRA

P24: [April 2018] [**Claims Journal**] [**science@ASU**] [**Office of Applied Innovation, ASU**][**Insurance Journal**]
Researcher Says Autonomous Vehicles Are Traveling the Wrong Road to Safety
Autonomous vehicles traveling the wrong road to safety, engineer says
Autonomous vehicles traveling the wrong road to safety, engineer says

P23: [April 2018] [**NPR-KJZZ**]
The Show: Aviral's interview on Should Autonomous Car Makers Slow Down Testing?

P22: [March 2018] [**NewsWise**]
Arizona State University professor asks, 'Why we would try to simulate human driving in AVs, when human driving is inherently flawed?'

P21: [March 2018] [**Insurance Journal**]
Human Influence makes Autonomous Vehicles Programming Unsafe

P20: [May 2017] [**Squire Patton Boggs**]
Aviral joins a Panel Discussion on "Autonomous Vehicles: Is our Infrastructure Ready?"

P19: [December 2017] [**FreePressJournal**]
Aviral gives Keynote on "Time in Cyber-Physical Systems" at IEEE-iNIS

P18: [July 2016] [**KTAR News**]
Arizona universities drawing in technology companies.

P17: [June 2016] [**ASU Full Circle**]
Expect the Unexpected: Autonomous car project prepares engineers for industry challenges

P16: [April 2016] [**The State Press**]
Robotics from A to Z

P15: [April 2016] [**ASU Full Circle**] [**Fulton Magazine**]
Robotic autonomous cars teach whole system design
Robotic autonomous cars teach whole system design

P14: [December 2015] [**NSF**]
An Elevator Pitch: Real People, Real Elevators

P13: [May 2014] [**Embedded Computing**]
Accelerating processing with Coarse Grain Reconfigurable Arrays

P12: [July 2013] **[The State Press]**
Robot car steers engineering students' future

P11: [July 2013] **[RobAid]**
Infinibotics Cosmo: Robotic toy car meant for edutainment

P10: [July 2013] **[ASU Now]**
Robotic toy car drives engineering students business venture

P9: [October 2012] **[ASU Inner Circle]**
Creative teaching approaches put spotlight on ASU engineers

P8: [February 2012] **[ASU Full Circle]**
Aviral was awarded the NSF Career Award to support his research on the reliable computing

P7: [February 2012] **[ASU Full Circle]**
Our research on reliability

P6: [January 2012] **[The State Press]**
ASU Technology Team Prepares for Shanghai

P5: [October 2011] **[ASU Full Circle]**
Advances in reliable computing draw recognition for doctoral student

P4: [April 2011] **[The State Press]**
Intel Corp. facility opens opportunity for students

P3: [January 2011] **[Intel]**
Arizona state university & Intel Corporation collaboration in parallel computing

P2: [August 2008] **[ASU Full Circle]**
Science Foundation Arizona grant to ASU/Raytheon Research Group will fund effort to expand computer capabilities

P1: [September 2007] **[Microsoft Research]**
Compiler and Microarchitectural Techniques for Leakage Power Reduction

PROFESSIONAL ACTIVITIES AND SERVICE

Summary of professional activities and service

Highlights:

- **Chair of the CS Graduate Program** at the School of Computing and AI @ ASU.
- **Editor-in-Chief** for IEEE Embedded Systems Letters (IEEE ESL) 2024-2028.
- **General Chair** of LCTES (Languages Compilers Tools and Theory for Embedded Systems) 2024.
- **Track Chair** of Autonomous Systems in Design Automation Conference (DAC) 2024 and 2025.
- **Steering Committee Member** of ESWEEK 2023, CODES+ISSS 2023, and LCTES 2018-2023
- **General Chair** of Embedded Systems Week 2022.
- **Deputy Editor-in-Chief** for IEEE Embedded Systems Letters (IEEE ESL) 2019-2023
- **Associate Editor** for ACM Transactions Embedded Computing Systems (ACM TECS), ACM Transactions on Cyber-Physical Systems (ACM TCPS) and Springer International Journal on Parallel Processing (Springer IJPP).
- **Technical Program Chair** for International Conference on Hardware Software Codesign and System Synthesis (CODES+ISSS) 2017, and 2018, and for Languages Compilers Tools, and Theory for Embedded Systems (LCTES) 2019, and Design and Applications track chair at Real-Time Systems Symposium (RTSS) 2020.
- **General Chair** of DAC Early Career Workshop (DAC-ECW) in 2017 and 2018, International Workshop on Cross-Layer Resilience (IWCR) 2017, Compiler-Assisted SoC Assembly (CASA) workshop from 2011-2014.

Editor-in-Chief

- 2025
    a. Editor-in-Chief of IEEE ESL (Embedded Systems Letters)
- 2024
    b. Editor-in-Chief of IEEE ESL (Embedded Systems Letters)
- 2023
    a. Deputy Editor-in-Chief of IEEE ESL (Embedded Systems Letters)
- 2022
    a. Deputy Editor-in-Chief of IEEE ESL (Embedded Systems Letters)
- 2021
    a. Deputy Editor-in-Chief of IEEE ESL (Embedded Systems Letters)
- 2020
    a. Deputy Editor-in-Chief of IEEE ESL (Embedded Systems Letters)

Associate Editor for peer reviewed journals

- 2025
    a. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
    b. Associate Editor for ACM TCPS (Transactions on Cyber-Physical Systems)
    c. Associate Editor for Springer IJPP (International Journal for Parallel Processing)
- 2024
    d. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)

e. Associate Editor for ACM TCPS (Transactions on Cyber-Physical Systems)
f. Associate Editor for IEEE TCAD (Transactions on Computer-Aided Design)
g. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2023
  a. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
  b. Associate Editor for ACM TCPS (Transactions on Cyber-Physical Systems)
  c. Associate Editor for IEEE TCAD (Transactions on Computer-Aided Design)
  d. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)
  e. Associate Editor for Springer IJPP (International Journal for Parallel Processing)
- 2022
  a. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
  b. Associate Editor for ACM TCPS (Transactions on Cyber-Physical Systems)
  c. Associate Editor for IEEE TCAD (Transactions on Computer-Aided Design)
  d. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)
  e. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2021
  a. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
  b. Associate Editor for IEEE TCAD (Transactions on Computer-Aided Design)
  c. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)
  d. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2020
  a. Guest Editor for ACM TCPS (Transactions on Cyber-Physical Systems)
  b. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
  c. Associate Editor for IEEE TCAD (Transactions on Computer-Aided Design)
  d. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)
  e. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2019
  a. Guest Editor for ACM TCPS (Transactions on Cyber-Physical Systems)
  b. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
  c. Associate Editor for IEEE TCAD (Transactions on Computer-Aided Design)
  d. Associate Editor for IEEE TMSCS (Transactions on MultiScale Computing Systems)
  e. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)
  f. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2018
  a. Guest Editor for ACM TCPS (Transactions on Cyber-Physical Systems)
  b. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
  c. Associate Editor for IEEE TCAD (Transactions on Computer-Aided Design)
  d. Associate Editor for IEEE TMSCS (Transactions on MultiScale Computing Systems)
  e. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)
  f. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2017
  a. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
  b. Associate Editor for IEEE TMSCS (Transactions on MultiScale Computing Systems)
  c. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)

d. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2016
    a. Associate Editor for ACM TECS (Transactions on Embedded Computing Systems)
    b. Associate Editor for IEEE TMSCS (Transactions on MultiScale Computing Systems)
    c. Associate Editor for Springer DAEM (Design Automation for Embedded Systems)
    d. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

- 2015
    a. Associate Editor for Springer IJPP (International Journal for Parallel Processing)

Conference/Workshop Organization

- 2024
    a. **[DAC]** Track Chair for Autonomous Systems
    b. **[ESWEEK]** Member of Steering Committee
    c. **[CODES+ISSS]** Member of Steering Committee
    d. **[LCTES]** Member of Steering Committee

- 2024
    a. **[LCTES]** General Chair
    b. **[DAC]** Track Chair for Autonomous Systems
    c. **[ESWEEK]** Member of Steering Committee
    d. **[CODES+ISSS]** Member of Steering Committee
    e. **[LCTES]** Member of Steering Committee

- 2023
    a. **[ESWEEK]** Member of Steering Committee
    b. **[CODES+ISSS]** Member of Steering Committee
    c. **[LCTES]** Member of Steering Committee

- 2022
    a. **[ESWEEK] General Chair** of ESWEEK 2022
    b. **[LCTES]** Member of Steering Committee

- 2021
    a. **[ESWEEK 2021]** Vice General Chair of ESWEEK 2021
    b. **[LCTES 2021]** Member of Steering Committee

- 2020
    a. **[ESWEEK 2020]** Virtual Conference Chair of ESWEEK
    b. **[ESWEEK 2020]** SIGDA representative to ESWEEK
    c. **[RTSS 2020]** Track Chair of Design and Application track (1/2 of RTSS)
    d. **[LCTES 2020]** Member of Steering Committee

- 2019

a. **[LCTES 2019]** Chair of the Technical Program Committee for the Languages, Compilers, Tools and Theory for Embedded Systems.
b. **[ESWEEK 2019]** SIGDA representative to ESWEEK

- 2018
  a. **[DAC ECW]** Program co-chair of the 2018 DAC Early Career Workshop
  b. **[CODES+ISSS]** Chair of the Technical Program Committee for the International symposium on Hardware/Software Codesign and System Synthesis.

- 2017
  a. **[DAC ECW]** Program co-chair of the 2017 DAC Early Career Workshop
  b. **[IWCR]** Program co-chair of the 2017 International Workshop on Cross-Layer Reliability
  c. **[CODES+ISSS]** Co-chair of the Technical Program Committee for the International symposium on Hardware/Software Codesign and System Synthesis.
  d. **[DATE]** Chair for the "Embedded Software" track at DATE 2017.

- 2016
  a. **[ESWEEK]** Web Chair of ESWEEK 2016.
  b. **[CODES+ISSS]** Track-chair of the "Embedded Software" track at CODES+ISSS.

- 2015
  a. **[ESWEEK]** Web Chair of ESWEEK 2015.

- 2014
  a. **[ESWEEK]** Web Chair of ESWEEK 2014.
  b. **[CASA]** Co-chair of the Workshop on Compiler Aided System-on-Chip Assembly

- 2013
  a. **[ESWEEK]** Web Chair of Embedded Systems Week, the top embedded systems event.
  b. **[CASA]** Co-chair of the Workshop on Compiler Aided System-on-Chip Assembly

- 2012
  a. **[CASA]** Co-chair of the Workshop on Compiler Aided System-on-Chip Assembly
  b. **[ESWEEK]** Web Chair of Embedded Systems Week, the top embedded systems event.
  c. **[PRIME]** Co-chair of the workshop on "Power and Reliability Issues in Multicore Era"

- 2011
  a. **[CASA]** Co-chair of the Workshop on Compiler Aided System-on-Chip Assembly
  b. **[ESWEEK]** Web Chair of Embedded Systems Week, the top embedded systems event.

- 2010
  a. **[ESWEEK]** Web Chair of Embedded Systems Week, the top embedded systems event.
  b. **[LCTES]** Organized Poster Session and Works-in-Progress session, at Languages Compilers and Tools for Embedded Systems.
- 2009
  a. **[LCTES]** Organize Poster Session and Works-in-Progress session, at the International Conference on Languages Compilers and Tools for Embedded Systems.

Technical Program Committee Membership

- 2025
    a. **[DAC]** Design Automation Conference
    b. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    c. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
- 2024
    a. **[DAC]** Design Automation Conference
    b. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    c. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems

- 2023
    a. **[DAC]** Design Automation Conference
    b. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    c. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems

- 2022
    a. **[RTAS]** Real Time and Embedded Technology and Applications Symposium
    b. **[DAC]** Design Automation Conference
    c. **[ASPDAC]** Asia South-Pacific Design Automation Conference
    d. **[ICCD]** International Conference on Computer Design

- 2021
    a. **[ICASSP]** International Conference on Acoustics, Speech and Signal Processing
    b. **[RTAS]** Real Time and Embedded Technology and Applications Symposium
    c. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    d. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    e. **[ICASSP]** International Conference on Acoustics, Speech and Signal Processing
    f. **[FCCM]** International Symposium on Field-Programmable Custom Computing Machines
    g. **[ICCD]** International Conference on Computer Design
    h. **[DSD]** Digital System Design

- 2020
    a. **[ICASSP]** International Conference on Acoustics, Speech and Signal Processing
    b. **[RTAS]** Real Time and Embedded Technology and Applications Symposium
    c. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
    d. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    e. **[ICASSP]** International Conference on Acoustics, Speech and Signal Processing
    f. **[FCCM]** International Symposium on Field-Programmable Custom Computing Machines

g. **[ICCD]** International Conference on Computer Design
h. **[DSD]** Digital System Design

- 2019
  a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
  b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
  c. **[FCCM]** International Symposium on Field-Programmable Custom Computing Machines
  d. **[ICCD]** International Conference on Computer Design
  e. **[VLSID]** International Conference on VLSI Design

- 2018
  a. **[DAC]** Design Automation Conference
  b. **[VLSID]** International Conference on VLSI Design

- 2017
  a. **[DAC]** Design Automation Conference
  b. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
  c. **[VLSID]** International Conference on VLSI Design

- 2016
  a. **[LCTES]** Languages Compilers and Tools for Embedded Systems
  b. **[ICCAD]** International Conference on Computer Aided Design
  c. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
  d. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
  e. **[EMSOFT]** International Conference on Embedded System Software
  f. **[VLSID]** International Conference on VLSI Design

- 2015
  a. **[LCTES]** Languages Compilers and Tools for Embedded Systems
  b. **[ICCAD]** International Conference on Computer Aided Design
  c. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
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f. **[RTCSA]** International Conference on Embedded and Real-Time Computing Systems and Applications

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    c. **[DSD]** Euromicro Conference on Digital System Design

- 2011
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    c. **[LCTES]** International Conference on Languages Compilers and Tools for Embedded Systems
    d. **[RTCSA]** International Conference on Embedded and Real-Time Computing Systems and Applications
    e. **[DSD]** Euromicro Conference on Digital System Design
    f. **[VLSID]** International Conference on VLSI Design

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- 2007
  a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems

Session Chair at Conferences

- 2025
  a. **[CODES+ISSS]** International Conference on Co-design and System Synthesis

- 2024
  a. **[VTS]** VLSI Test Symposium
  b. **[CODES+ISSS]** International Conference on Co-design and System Synthesis

- 2023
  a. **[CODES+ISSS]** International Conference on Co-design and System Synthesis

- 2020
  a. **[DAC]** Design Automation Conference

- 2019
  a. **[VLSID]** International Conference on VLSI Design
  b. **[ESWEEK]** Embedded Systems Week
  c. **[DAC]** Design Automation Conference

- 2018
  a. **[DAC]** Design Automation Conference

- 2017
  a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems

- 2016

a. **[DAC]** Design Automation Conference
b. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis
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    c. **[LCTES]** International Conference on Languages Compilers and Tools for Embedded Systems

- 2008
    a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems

- 2007
    a. **[CASES]** International Conference on Compilers Architectures and Synthesis of Embedded Systems
    b. **[ISLPED]** International Symposium on Low Power Electronic Design

- 2006
    a. **[CODES+ISSS]** International Conference on Hardware-Software Codesign and System Synthesis

Journal Refereeing

- **[IEEE TPDS]** IEEE Transactions on Parallel and Distributed Systems
- **[IEEE TCAD]** IEEE Transactions on Computer Aided Design
- **[IEEE TVLSI]** IEEE Transactions on Very Large Integrated Circuits
- **[ACM TC]** ACM Transactions on Computing
- **[ACM TACO]** ACM Transactions on Architectures and Code Optimization
- **[ACM TODAES]** ACM Transactions on Design and Analysis of Embedded Systems
- **[IJPP]** Springer International Journal on Parallel Processing

Professional Society Membership

- Association of Computing Machinery (ACM) – Lifetime member
- Institute for Electrical and Electronic Engineers (IEEE) – Senior Member

UNIVERSITY SERVICE

University Committees

- 2019
    a. CISDE Representative to the ASU Senate

- 2018
    a. CISDE Representative to the ASU Senate

- 2017
    a. CISDE Representative to the ASU Senate

Department Committees

- 2024
    a. Graduate Program Chair
    b. Ex-officio member of Graduate Program Committee
    c. Ex-officio member of Administration and Planning Committee

- 2024
    a. Graduate Program Chair
    b. Ex-officio member of Graduate Program Committee
    c. Ex-officio member of Administration and Planning Committee

- 2023
    a. Graduate Program Chair
    b. Ex-officio member of Graduate Program Committee
    c. Ex-officio member of Administration and Planning Committee

- 2022
    a. Computer Science and Engineering Administration and Planning Committee
    b. Computer Engineering Graduate Program Committee
    c. Computer Science and Engineering Graduate Program Committee

- 2021
    a. Computer Science and Engineering Personnel Committee
    b. Computer Engineering Graduate Program Committee
    c. Computer Science and Engineering Graduate Program Committee

- 2020
    a. Computer Science and Engineering Personnel Committee
    b. Computer Engineering Admissions Committee
    c. Computer Engineering Graduate Program Committee

- 2019
    a. Computer Science and Engineering Personnel Committee
    b. Computer Science and Engineering Graduate Program Committee
    c. Computer Engineering Admissions Committee
    d. Computer Engineering Graduate Program Committee

- 2018
    a. Computer Science and Engineering Graduate Program Committee
    b. Computer Engineering Admissions Committee
    c. Computer Engineering Graduate Program Committee

- 2017
    a. Computer Science and Engineering Graduate Program Committee
    b. Computer Engineering Admissions Committee

c. Computer Engineering Graduate Program Committee

- 2016
  a. Computer Science and Engineering Graduate Program Committee
  b. Chair of Computer Engineering Admissions Committee
  c. Chair of Computer Engineering Graduate Program Committee

- 2015
  a. Computer Science and Engineering Graduate Program Committee
  b. Chair of Computer Engineering Admissions Committee
  c. Chair of Computer Engineering Graduate Program Committee

- 2014
  a. Computer Science and Engineering Graduate Program Committee
  b. Chair of Computer Engineering Admissions Committee

- 2013
  a. on sabbatical

- 2012
  a. Computer Science and Engineering Graduate Program Committee
  b. Computer Science and Engineering Undergraduate Program Committee

- 2011
  a. Computer Science and Engineering Graduate Program Committee
  b. Computer Science and Engineering Undergraduate Program Committee

- 2010
  a. Computer Science Undergraduate Program Committee
  b. Computer Science and Engineering Graduate Program Committee

- 2009
  a. Graduate Admissions Committee

- 2008
  a. Graduate Admissions Committee
  b. Computing Resources Committee

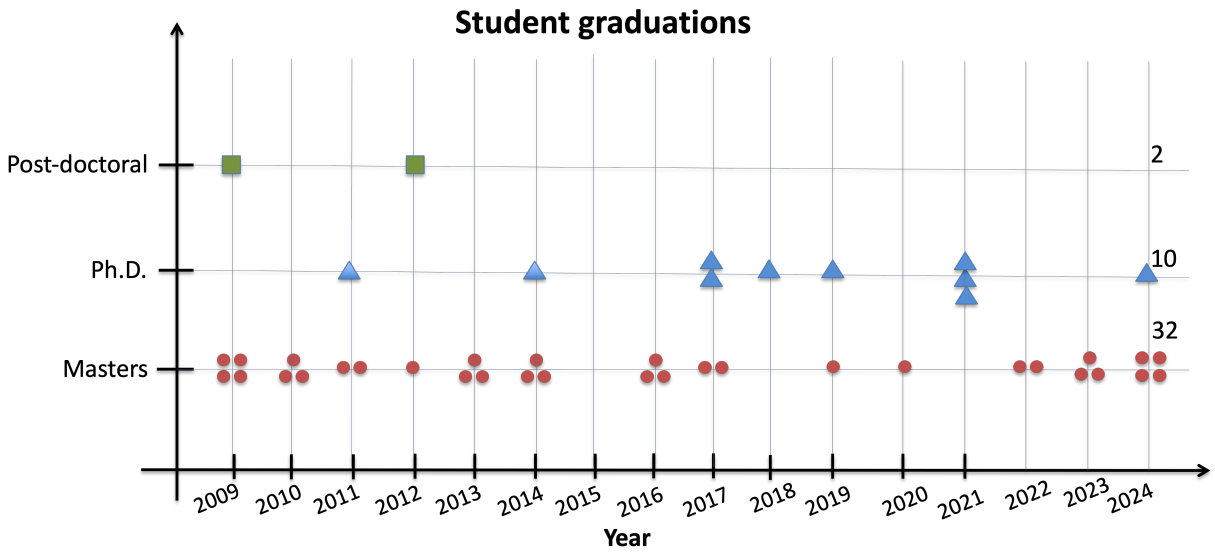
- 2007
  a. Graduate Admissions Committee

- 2006
  a. Graduate Admissions Committee

STUDENT MENTORING, TEACHING AND OUTREACH

Highlights of mentoring, teaching and outreach

- **Graduated** 2 post-docs, 10 Ph.Ds., and 32 Computer Science Masters students.
- 2 of my students are in **Academia**.
- 2 of my Ph.D. students have received **Outstanding Computer Engineering Ph.D. Dissertation Award**.
- 3 of my master's students have received **Outstanding Computer Engineering Master's Dissertation Award**.
- Supervised **5 Honors Undergraduate thesis.**
- Coordinated and taught 3 **professional courses.**



Post-doctoral Candidates

PD3. **Hwisoo So** *(*Fall 2023 - ongoing)
Topic: Reliability of Machine Learning Models.

PD2. **Reiley Jeyapaul** *(*Spring 2012 - Fall 2012)
Current employment: ARM Research, Cambridge, UK

PD1. **Jongeun Lee** (Fall 2007 - Spring 2009)
Currently: Assistant Professor at UNIST, South Korea.

Graduated Ph.D. Students

GP10. **Shail Dave,** Computer Engineering, graduated Summer 2024.

Thesis: **An Agile Methodology for Designing Efficient Domain-Specific Architectures**
Employment: Qualcomm Inc., San Diego, CA, USA.

GP9. **Mahesh Balasubramanian,** Computer Engineering, graduated Summer 2021.
Thesis: Compiler Design for Accelerating Applications on Coarse-Grained Reconfigurable Architectures
Employment: Qualcomm Inc., San Diego, CA, USA.

GP7. **Mohammad Khayatian,** Computer Engineering, Summer 2020.
Thesis: Safe and Robust Cooperative Algorithms for Connected Autonomous Vehicles
(Outstanding Computer Engineering Ph.D. Dissertation Award)
Employment: Vecna Robotics, Boston, MA

GP8. **Mohammadreza Mehrabian,** Computer Engineering, graduated Spring 2019.
Thesis: A Methodology and Formalism to Monitor Timing Specifications Of Cyber-Physical Systems
Employment: Assistant Professor, South Dakota School of Mines and Technology, Rapid City, SD, USA.

GP6. **Jing Lu,** Computer Science, Spring 2019.
Thesis: Application-aware Performance Optimization for Software Managed Manycores.
Employment: Apple Inc., Cupertino, USA.

GP5. **Moslem Didehban,** Computer Engineering, Fall 2018.
Thesis: *Software Techniques for Soft Error Resilience*.
Employment: Nvidia, Santa Clara, USA.

GP4. **Jian Cai,** Computer Science, Fall 2017.
Thesis: *Communication Management in Distributed Memory Multi-core Processors*.
Employment: Google, Sunnyvale, CA, USA.

GP3. **Yooseong Kim,** Computer Science, Spring 2017.
Thesis: *WCET-Aware Scratchpad Memory Management for Hard Real-Time Systems*.
(Outstanding Computer Engineering Dissertation Award)
Employment: Mercedes Benz Research, San Jose, CA, USA.

GP2. **Ke Bai,** Computer Science, Spring 2014.
Thesis: *Compiler and Runtime for Memory Management on Software Managed Manycore Processors*.
Employment: Google, Sunnyvale, CA, USA.

GP1. **Reiley Jeyapaul***,* defended his thesis in Fall 2011
Thesis: Smart Compilers for Reliable and Power-efficient Embedded Computing
Employment: RAS Architect, Nvidia, Austin, TA, USA.

Current PhD Students

CP4. **Vinayak Sharma,** Computer Science, Fall 2024 – present.
Thesis: *Quantum Machine Learning*
Status: Expected graduation: Fall 2028

CP3. **Atharva Khedkar,** Computer Science, Fall 2023 – present.
Thesis: *Multi-Level Intermediate Representation*
Status: Expected graduation: Fall 2028

CP2. **Adam Awale,** Computer Engineering, Fall 2022 – present.
Thesis: *Accelerated Computing*
Status: Expected graduation: Spring 2028

CP1. **Edward Andert,** Computer Engineering, Fall 2019 – present.
Thesis: *Autonomous Vehicles*
Status: Expected graduation: Fall 2025

Graduated Master's Students

GM32. **Sumedh Joshi**, Computer Science, Fall 2024
Thesis: ProGIP: Protecting Gradient-based Input Perturbation Approaches for Out-of-distribution Detection from Soft Errors
Employment: Entrepreneur

GM31. **Francis Mendoza**, Computer Science, Fall 2024
Thesis: AEGIS: A Special-Purpose Computer Network for Strategic Cyber Defense
Employment: Entrepreneur

GM30. **Abhinav Kumar**, Computer Science, Fall 2024
Thesis: DSP-MLIR: A Compiler for Digital Signal Processing in MLIR
Employment: Entrepreneur

GM29. **Sai Shashank Peddiraju**, RAS, Summer 2024
Thesis: IncidentNet: Traffic Incident Detection, Localization and Severity Estimation with Sparse Sensing
Employment: Amazon Web Services

GM28. **Guna Lagudu**, Computer Science, Summer 2024
Thesis: LUCI: Multi-Application Orchestration Agent
Employment: Entrepreneur

CM27. **Vinayak Sharma**, Computer Science, Spring 2024
Research topic: Quantum Polar Metric Learning: Efficient Classically Learned Quantum Embeddings
Employment: Ph.D. in CS@ASU.

GM26. Shreehari Jagadeesha, Computer Engineering, Fall 2023
Thesis: TIPANGLE: A Machine Learning Approach for Accurate Spatial Pan and Tilt Angle Determination of Pan Tilt Traffic Cameras
Employment: Entrepreneur

GM25. Matthew Szeto, Computer Engineering, Spring 2023
Thesis: B-AWARE: Blockage Aware RSU Scheduling for 5G Enabled Autonomous Vehicles
Employment: Intel, Chandler

GM24. Quoc Long Vinh Ta, Computer Engineering, Fall 2022
Thesis: COMSAT: Modified Modulo Scheduling Techniques for Acceleration of Unknown Trip Count and Early Exit Loops
Employment: Ph.D. student at ASU

GM23. Sanggu Park, Computer Engineering, Summer 2022
Thesis: Blame-Free Motion Planning in Hybrid Traffic
Outstanding Computer Engineering Master's thesis Award
Employment: Signals Officer, Republic of Korea Army.

GM22. Harshith Alamsetti, Computer Engineering, Spring 2020
Thesis: Cooperative Driving of Connected Autonomous Vehicles Using Responsibility Sensitive Safety Rules
Employment: Western Digital Inc., Milpitas, CA.

GM21. Rachel Dedinsky, Computer Engineering, Spring 2019
Thesis: R2IM: Reliable and Robust Intersection Management of Connected Autonomous Vehicles
Employment: Apple, Seattle, WA.

GM20. Jinn-Pean Lin, Computer Science, graduated Summer 2017
Research topic: Optimizing Heap Data Management on Software Managed Manycores
Employment: forcepoint, Campbell CA.

GM19. Edward Andert, Computer Engineering, graduated Spring 2017
Thesis: Crossroads - A Time-Sensitive Autonomous Intersection Management Technique
Employment:

GM18. Dheeraj Lokam, Computer Science, graduated Fall 2016
Thesis: InCheck - An Integrated Recovery Methodology for Fine-grained Soft-Error Detection Schemes
Employment: Intel, Chandler, AZ.

GM17. Shail Dave, Computer Science, graduated Fall 2016
Thesis: Scalable Register File Architecture for CGRA Accelerators
Employment: continuing with Ph.D. at ASU.

GM16. Karthik Tanikella, Computer Science, graduated in Spring 2016
Thesis: gemV: A Validated Model to Estimate Architectural Vulnerability
Employment: Axys Automation, Phoenix, AZ, USA.

GM15. **Tushar Rawat,** Computer Science, graduated in Fall 2014
Thesis: Enabling Multithreaded Applications on Hybrid Shared Memory Many-core Architectures
Employment: Tesla Motors, CA, USA.

GM14. **Shri Rajendran Radhika,** Computer Science, graduated in Fall 2014
Thesis: Path Selection Based Branching for Coarse Grained Reconfigurable Arrays
Employment: Intel, Chandler, AZ, USA.

GM13. **Dipal Singh,** Computer Science, Spring 2014
Research topic: Register File Organization for Coarse-Grained Reconfigurable Architectures
Employment: Mathworks, Nattick, MA, USA.

GM12. **Russel Dill,** Computer Science, Fall 2013
Thesis: Integrated Design of flash translation layer and flash file system.
Employment: Texas Instruments.

GM11. **Bryce Holton,** Computer Science, Fall 2013
Thesis: GCCFG: A novel graph representation for Inter-procedural Optimizations.
Employment: Alaris, Phoenix, AZ, USA.

GM10. **Abhishek Rhisheekesan,** graduated in Spring 2013
Thesis: Quantitative Evaluation of Control-flow based Soft Error Protection Mechanisms.
Outstanding Computer Engineering Master's thesis Award
Employment: Intel, Bangalore, India.

GM9. **Di Lu,** graduated in Spring 2012
Thesis: Vector Class on Limited Local Memory Multi-core Processors.
Employment: Alcatel-Lucent, San Jose, CA.

GM8. **Jared Pager**, graduated in Fall 2011
Thesis: Increasing CGRA Utilization through Multi-threading for Power-efficient Embedded Systems
Employment: Intel, Portland, OR.

GM7. **Fei Hong**, graduated in Spring 2011
Thesis: UnSync: A Soft-Error Resilient Redundant CMP Architecture
Employment: Allied Telesis, San Jose, CA.

GM6. **Saleel Kudchadker**, graduated in Fall 2010
Thesis: Managing Stack Data on Limited Local Memory Multi-core Architectures
Employment: AMD, Sunnyvale, CA.

GM5. **Seung-chul Jung**, graduated in Spring 2010
Thesis: Dynamic Code Mapping for Limited Local Memory Architectures
Outstanding Computer Engineering Master's thesis Award
Employment: Custom Sensors and Technology, Concord, CA.

GM4. **Sai Mylavarapu**, graduated in Spring 2009

Thesis: Improving Application Response Times of Nand Flash based Systems
First employment: Micron, Milpitas, CA.

GM3. **Rooju Chokshi**, graduated in Spring 2009
Thesis: Residue number system enhancements for programmable processors
First employment: Microsoft, Redmond, WA.

GM2. **Amit Pabalkar**, graduated in Fall 2009
Thesis: A Dynamic Code Mapping Technique for Scratch Pad Memories in Embedded Systems
Employment: Nvidia, Santa Clara, CA.

GM1. **Arun Kannan**, graduated in Fall 2009
Thesis: A Software-Only Solution for Stack Management on Systems with Scratch Pad Memory
Employment: Apple Cupertino, CA.

Current Masters Students

CM7. **Rishab Kashyap**, Computer Science, Fall 2022 – present
Research topic: ML Acceleration
Expected graduation: Fall 2025.

CM6. **Kaustubh Harapanahalli**, Computer Science, Fall 2022 – present
Research topic: Advanced Manufacturing
Expected graduation: Spring 2025.

CM5. **Aman Singh**, Computer Science, Fall 2023 – present
Research topic: Reliability of ML Models
Expected graduation: Fall 2025.

CM4. **Ameya Gurjar**, Computer Science, Fall 2024 – present
Research topic: MLIR
Expected graduation: Fall 2025.

CM3. **Curt John Bansil**, Computer Science, Fall 2024 – present
Research topic: MLIR
Expected graduation: Fall 2025.

CM2. **Megan Kuo**, Computer Science, Fall 2024 – present
Research topic: MLIR
Expected graduation: Fall 2026.

CM1. **Gyan Pratipat**, Computer Science, Fall 2024 – present
Research topic: QML
Expected graduation: Fall 2026.

Graduated Honors Thesis

HT5. Making a Real-Time Operating System for the Raspberry Pi 2B
Christian Cunningham, School of Mathematics and Statistical Sciences
Year: 2022

HT4. An IoT Solution to Air Quality Monitoring
Abrahm Philip Coury, Cody Gillespie, Computer Science and Engineering
Year: 2019

HT3. Using an Open-source Solution to Implement a Drone Cyber-Physical System
Rachel Dedinsky, Harrison James Lubbers, Computer Science
Year: 2018

HT2. Internet-of-Things for Pet-Care
Gabriela Phyllis Coote, Mechanical and Aerospace Engineering Program
Year: 2016

HT1. A Non-intrusive Unit Testing Framework for C using LLVM/Clang
Alexander Iadicicco, Computer Science
Year: 2015

Professional Courses

PC3. [ImmerseAI Course for Yonsei University Graduate students]
Course – immerseAI course for graduate students from Yonsei University through GOEEE.
Role – Organizer and Lead Instructor
Students – 20
When – Feb 2024

PC2. [IoT Expert Course to TMobile employees]
Course - Professional certification course to TMobile employees through GOEEE.
Role – Organizer and Lead Instructor
Students – 30 TMobile/Verizon employees
When – Dec 2020

PC1. [Professional Course on Multicore Programming]
Course – Multicore Programming.
Role – Organizer and Lead Instructor
Students – 30 software developers from various companies in Phoenix
When – Dec 2009